

# PRAGYAN AI

## Grow with Gyan

# PragyanAI – SILICONAI

NITK | Stanford Ignite / Seed Spark | IIMA (Business Strategy Communication) | SLP Fellow |  
25+ Years Product Exp | Tech Leadership | Serial Entrepreneur

**Autonomous AI-First Engineering Workflows for Semiconductor Design, Verification & Talent Development**  
Democratizing Silicon Innovation for a Self-Reliant, AI-Powered India



Year of Incorporation / Registration  
**2021**



Founder(s) & Location  
**Sateesh Ambesange & Uppin Rashmi**  
Bangalore, India



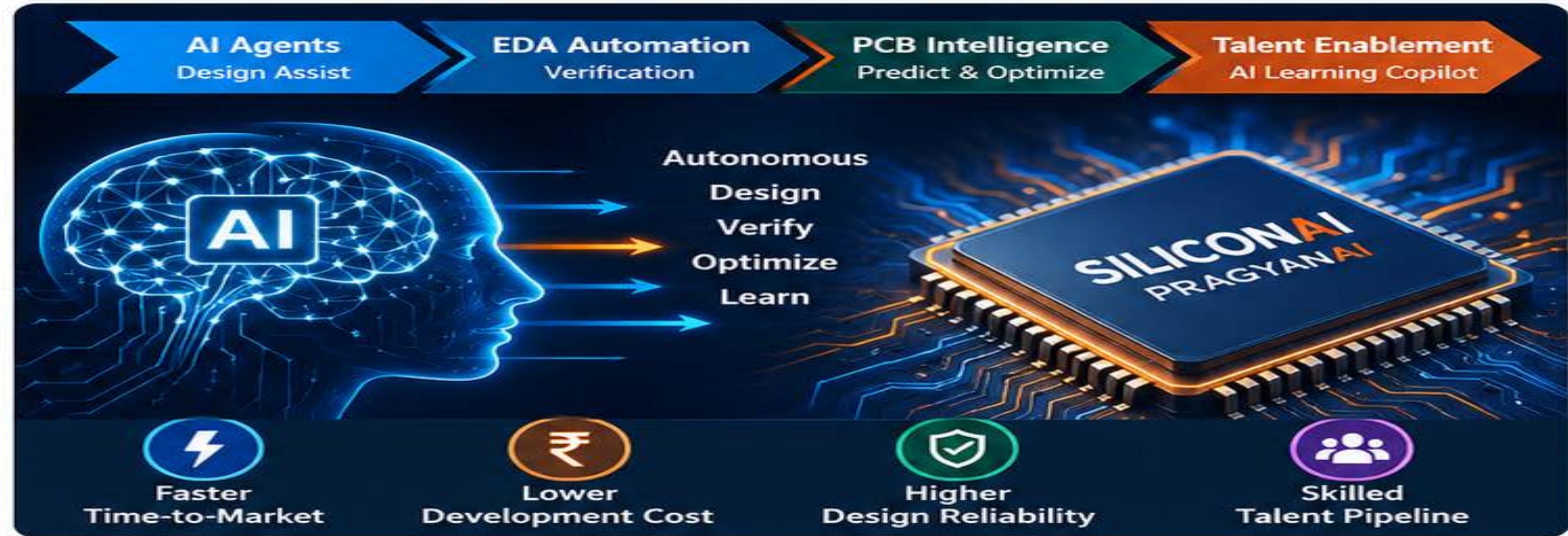
Website & Social Media Links  
[www.pragyansiliconai.com](http://www.pragyansiliconai.com)



Current Stage of Startup  
**TRL 4 : MVP**  
(Validated in Lab, Early Pilots)



Sector / Industry  
**Semiconductor | EDA | PCB | AI |  
DeepTech | Engineering Education**



## 12+ CORE SOLUTIONS

## AI-POWERED TOOLS FOR THE FULL SILICON & ELECTRONICS LIFECYCLE



**1. RTL Code Generator**  
AI-driven Verilog/SystemVerilog generation

Design Automation



**2. Testbench Synthesis**  
Automated UVM testbench generation

Verification



**3. AI Waveform Debugger**  
Root-cause analysis & waveform insights

Debug & Analysis



**4. Formal Verification Assistant**  
Property generation & formal checks

Verification



**5. PCB Design Copilot**  
AI-assisted schematic & layout design

PCB Design



**6. PCB DFM/DFT Analyzer**  
Predictive manufacturability & test analysis

PCB Intelligence



**7. Thermal & EMI Predictor**  
Pre-fabrication thermal and EMI analysis

Signal Integrity



**8. Hardware-Aware AI Compiler**  
Model quantization for edge silicon

Edge AI



**9. SoC Integration Assistant**  
IP integration & interface generation

SoC Design



**10. Silicon Verification Insights**  
Coverage, risk & quality analytics

Analytics



**11. Interactive Learning Copilot**  
AI tutor for VLSI/PCB/AI skills

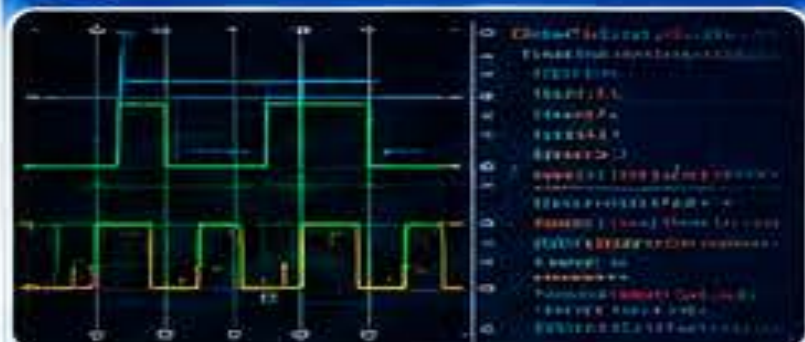
Talent Development



**12. Engineering Workflow Agent**  
End-to-end autonomous EDA workflows

Productivity

**1 Verification Bottleneck**



- Large design complexity
- Writing and maintaining testbenches
- Long simulation cycles
- Achieving coverage closure is hard

**40–60%**  
of engineering time spent on verification

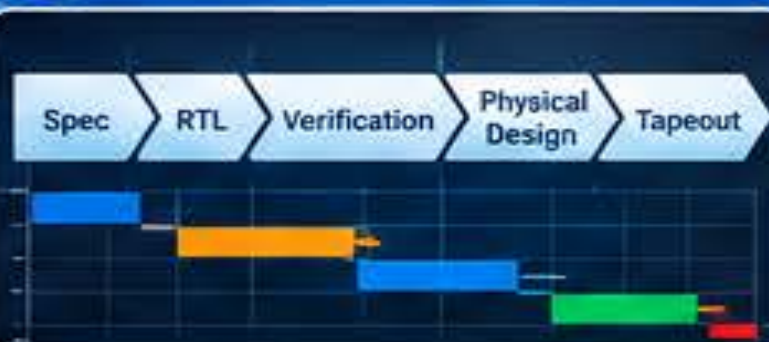
**2 Expensive EDA Tools**



- High license cost (multi-million \$)
- Complex to use and maintain
- Limited access for startups, MSMEs and academia

**\$1M – \$5M+**  
annual EDA tool cost for large projects

**3 Slow Development Cycles**



- Multiple iterations across stages
- Rework due to bugs and PPA issues
- Manual, expert-driven flow

**12 – 24+**  
months from specification to silicon

**4 Shortage of Expertise**



- Limited availability of experienced VLSI/PCB engineers
- High learning curve for EDA tools
- Growing demand for AI + semiconductor + systems skills

**Global talent gap ~1 Million+**  
semiconductor engineers by 2030 (industry estimates)

**5 Specification Ambiguity**



- Incomplete or unclear requirements
- Frequent clarifications and rework
- Misinterpretation leads to design errors later in the flow

**20–40%**  
design rework due to specification ambiguity

**6 Late Defect Discovery and Re-spin Cost**



- Bugs found late in physical design, silicon or board bring-up
- Re-spin is extremely costly and time consuming
- Impacts time-to-market and revenue

**\$1M – \$100M+**  
per re-spin (depending on technology)

**TRADITIONAL ENGINEERING FLOW**  
(Manual & Iterative)



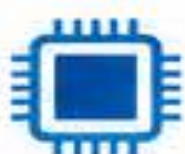
**High Cost  
Long Time  
Expert Dependent  
Multiple Iterations**

**AI-POWERED FLOW WITH SILICON AI**  
(Faster, Smarter, More Reliable)



**TARGET CUSTOMERS / USER SEGMENTS**

**Semiconductor Companies**



- IDMs
- Fabless design houses
- System companies

**High-value, core segment**

**Electronics & PCB Companies**



- Consumer electronics
- Industrial electronics
- Automotive electronics
- EMS / ODM / OEM

**Large and growing opportunity**

**Startups & MSMEs**



- Chip startups
- Product companies
- IoT, Automotive, Aerospace, Industrial

**Need cost-effective EDA + AI tools**

**Academia & Research Institutes**



- Universities
- Research labs
- Training & skilling programs

**Education, research and talent development**

**MARKET OPPORTUNITY (TAM / SAM / SOM)**



**TAM (Total Addressable Market)**

- Global EDA market ~\$14–18B (growing)
- Semiconductor design & verification services and related tools ecosystem ~\$100B+
- Broader electronics & PCB design ecosystem
- Estimated TAM: **\$130B+** (by 2030)

**SAM (Serviceable Available Market)**

- EDA + AI engineering tools for design, verification, PCB and systems
- Focus on fabless, EMS/OEM, automotive, industrial, consumer electronics, academia
- Estimated SAM: **\$20B+** (by 2030)

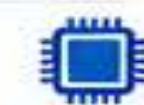
**SOM (Serviceable Obtainable Market)**

- Realistically target 5–10% of SAM in 5–7 years
- Estimated SOM: **\$1B – \$2B** (by 2030)

**MARKET DRIVERS**



Exploding semiconductor and electronics demand (AI, Automotive, IoT, 5G, Edge, HPC)



Increasing design complexity and time-to-market pressure



Rising cost and limited access to EDA tools



Shortage of experienced VLSI/PCB engineers



Need for AI-driven automation and productivity



Growing startup and MSME ecosystem

# PROBLEM 1: EXPENSIVE EDA & VERIFICATION

Advanced EDA is essential for chip and PCB development — but cost, complexity and tool fragmentation create a barrier for startups and MSMEs.

## 1 THE COST STACK

Multiple specialized tools, high license costs, compute infrastructure and expert engineering.

|                                                                                                                                                                            | Tool License Cost<br>(Annual, Illustrative Enterprise Range) | Engineering + Infrastructure Cost<br>(Annual, Illustrative)    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|----------------------------------------------------------------|
|  <b>RTL / Synthesis</b><br>Design & optimization<br>(Synopsys, Cadence, etc.)             | <b>\$10K – \$100K+</b><br>per tool / per seat                | <b>\$50K – \$200K+</b><br>(engineering effort, flows, support) |
|  <b>Simulation</b><br>Functional verification<br>(VCS, Xcelium, etc.)                     | <b>\$50K – \$300K+</b><br>per tool / per seat                | <b>\$100K – \$500K+</b><br>(run-time, compute, storage)        |
|  <b>Formal Verification</b><br>Property checking<br>(Formality, Jasper, etc.)             | <b>\$100K – \$500K+</b><br>per tool / per seat               | <b>\$100K – \$400K+</b><br>(expert engineers, flows)           |
|  <b>Physical Design</b><br>Place & route, timing<br>(ICC2, Innovus, etc.)                 | <b>\$100K – \$600K+</b><br>per tool / per seat               | <b>\$200K – \$800K+</b><br>(engineering effort, iterations)    |
|  <b>Sign-off / Verification</b><br>STA, DRC, LVS, SI, Power<br>(PrimeTime, Calibre, etc.) | <b>\$100K – \$600K+</b><br>per tool / per seat               | <b>\$200K – \$800K+</b><br>(sign-off, analysis, closure)       |
|  <b>Infrastructure &amp; Compute</b><br>Servers, storage, EDA cloud                       | —                                                            | <b>\$100K – \$500K+</b><br>(HPC servers, storage, IT admin)    |

 A complete, production-grade flow typically requires multiple tools, significant compute and a specialized team.

Ranges are illustrative and vary by vendor, seats, node, design size and specific use case.

## 2 WHY THIS BECOMES A STARTUP BARRIER

High cost, complexity and dependence on specialized expertise make advanced EDA inaccessible for many MSMEs and startups.

**1**  
**HIGH UPFRONT SPEND**  
**\$2M – \$10M**  
Typical annual cost for a small to mid-sized chip design team (10–50 engineers). Includes tools, compute and infrastructure.

**2**  
**MULTIPLE SPECIALIZED TOOLS**  
**6 – 15+**  
Different tools for design, simulation, formal, physical, sign-off, each with separate flows, licenses and learning curves.

**3**  
**SCARCE EXPERT ENGINEERS**  
**10 – 30x**  
Higher cost than open-source alternatives for similar functionality. Deep expertise required across digital, analog, timing, power, SI, etc.

**4**  
**TOOL INTEGRATION OVERHEAD**  
**20 – 40%**  
Of engineering time spent on tool setup, flow integration, format/debug issues instead of actual design innovation.

 A complete production flow can require **MULTIPLE SPECIALIZED EDA CATEGORIES + COMPUTE + EXPERT ENGINEERING.**



## 3 THE HIDDEN COST

It's not just license fees — it's engineer hours, infrastructure, delays and rework.



### Illustrative Scenario (Mid-size SoC / Advanced Node)

 **10–20 engineers**

Working across multiple tools and flows for 12–24 months

 **50K – 200K+ engineering hours**

Spent on setup, integration, simulation, debug and closure

 **6 – 18 months additional time**

Common due to tool learning, flow issues and iterative debug

### Real Impact

-  Higher upfront and ongoing costs
-  Longer time-to-market
-  Increased risk of design errors
-  Expensive rework or silicon respins
-  Diverts focus from product innovation

## 4 THE SILICONAI OPPORTUNITY

An AI-native engineering layer that works with your existing EDA tools.



### KEY BENEFITS

-  Reduce tool-operation overhead by 50–80%
-  Faster verification cycles (from weeks to days)
-  Make advanced capability accessible to smaller teams
-  Automate repetitive tasks and improve coverage
-  Leverage expert knowledge, anytime

# PROBLEM 2: SLOW DESIGN-TO-VERIFICATION CYCLES

End-to-end semiconductor / PCB development takes months to years, with verification as the biggest bottleneck.

## TRADITIONAL FLOW — MANUAL, TOOL-CENTRIC, SEQUENTIAL

Takes 12 – 24+ Months (Complex SoC)

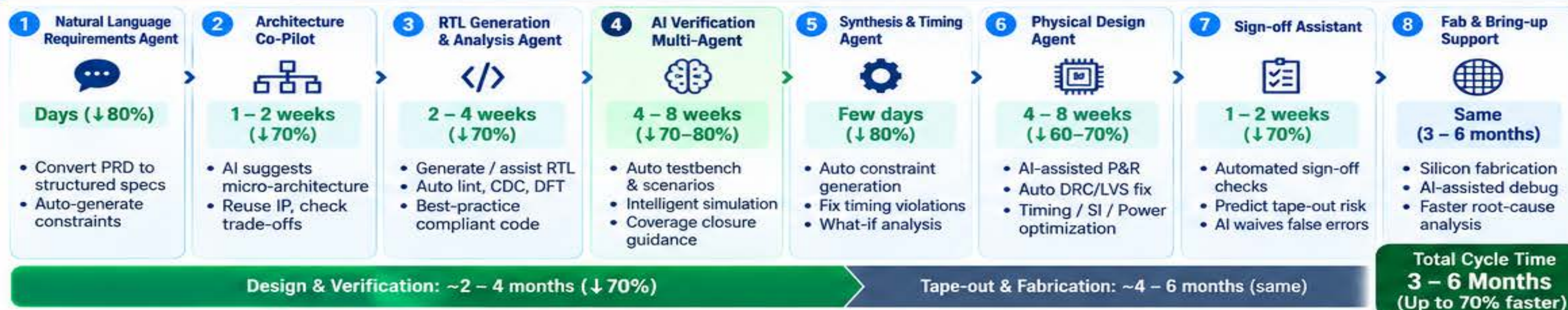


## KEY PAIN POINTS & DATA

- 70%** of development time spent in verification (Siemens EDA, 2023; EE Times)
- \$50M – \$200M** total cost for advanced EDA tool licenses per year (for a large design team) (Synopsys, Cadence, Siemens pricing)
- 6 – 15+** specialized tools required across the flow (Industry practice)

## AI-BASED FLOW WITH PRAGYANAI — INTELLIGENT, CONNECTED, AUTOMATED

Takes 3 – 6 Months (Complex SoC)



## ACCELERATION & COST REDUCTION

- 60 – 80%** faster verification cycles (Siemens, Cadence, Synopsys AI initiatives)
- 40 – 60%** lower EDA & compute costs (with optimized tool usage) (Industry analysis)
- 3 – 6×** higher engineer productivity (McKinsey, 2023 – GenAI in EDA)
- Lower re-spin risk** through early defect detection and AI-guided sign-off

## IMPACT OF LATE DEFECTS (WITHOUT AI)

The later a defect is found, the more it costs to fix.



## REAL-WORLD COST & TIME OF RE-SPINS

- \$5M – \$50M+** per silicon re-spin (cost depends on process node, e.g., 28nm–3nm) (SemiAnalysis, 2023)
- 6 – 12 months** additional time per re-spin (industry data)
- ~30 – 50%** of designs require at least one re-spin due to late-stage defects (IBS, 2023; industry surveys)

## END-TO-END COMPARISON (EXAMPLE: ADVANCED SOC)

| Metric                      | Traditional Flow                  | AI-Based (PragyanAI)                  | Improvement    |
|-----------------------------|-----------------------------------|---------------------------------------|----------------|
| Total Development Time      | 12 – 24 months                    | 3 – 6 months                          | ↓ 60 – 75%     |
| Verification Time (portion) | 70% of total                      | 15 – 25% of total                     | ↓ 70 – 80%     |
| EDA Tool & Compute Cost     | \$50M – \$200M+/year (large team) | \$20M – \$80M/year (optimized usage)  | ↓ 40 – 60%     |
| Engineer Productivity       | 1× (baseline)                     | 3 – 6×                                | ↑ 3 – 6×       |
| Re-spin Probability         | 30 – 50%                          | 10 – 20%                              | ↓ 50 – 70%     |
| Re-spin Cost (per event)    | \$5M – \$50M+                     | \$5M – \$50M+ (but lower probability) | ↓ overall risk |
| Time to Market              | 12 – 24 months                    | 3 – 6 months                          | ↓ 60 – 75%     |

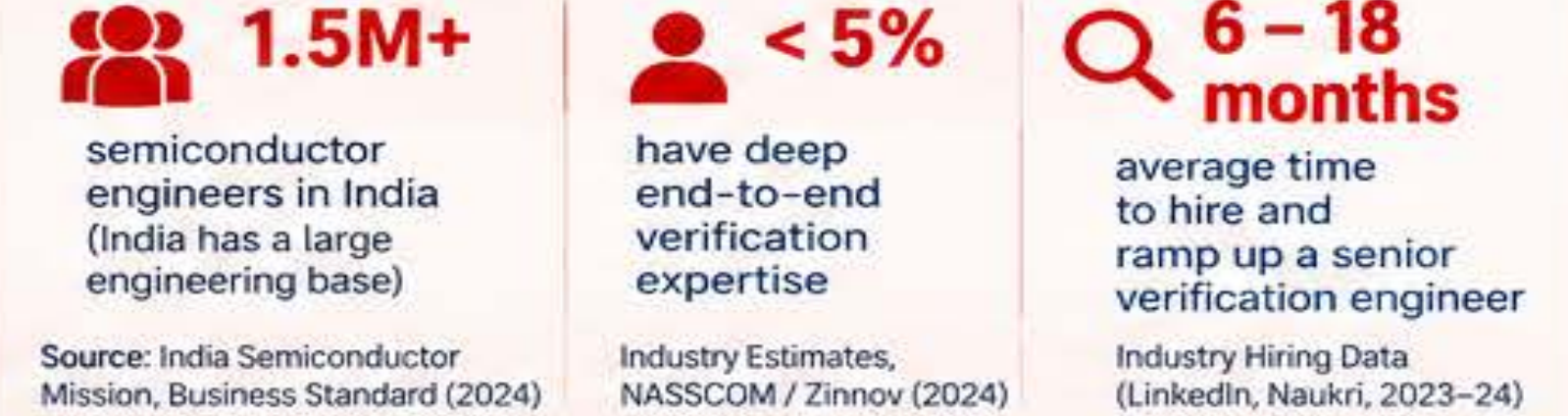
# PROBLEM 3: SCARCITY OF SPECIALIZED EXPERTISE

Verification requires deep, multi-domain expertise, which is scarce, expensive and hard to hire.

## VERIFICATION REQUIRES EXPERTISE ACROSS MULTIPLE DOMAINS



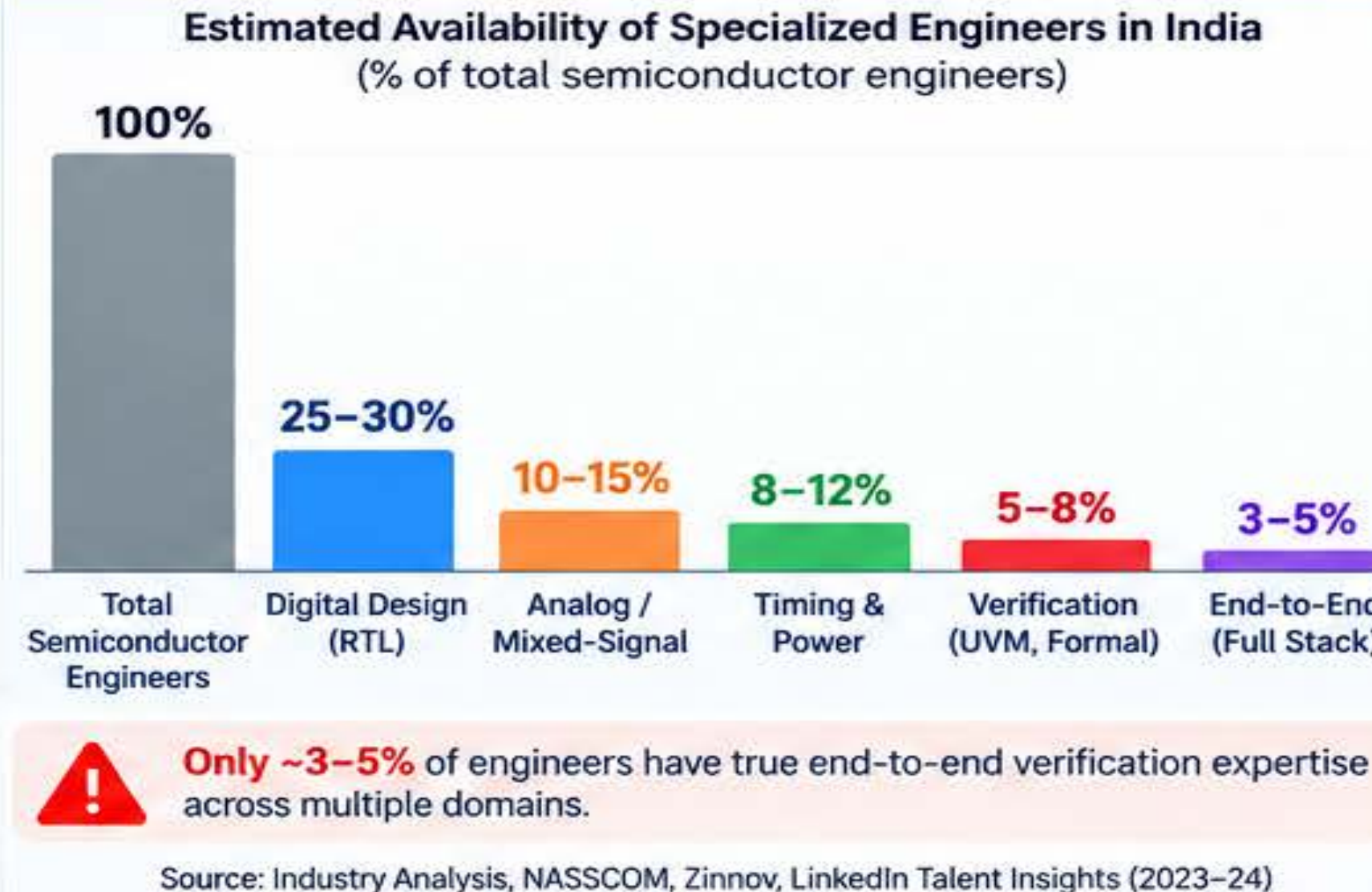
## THE TALENT GAP IS REAL



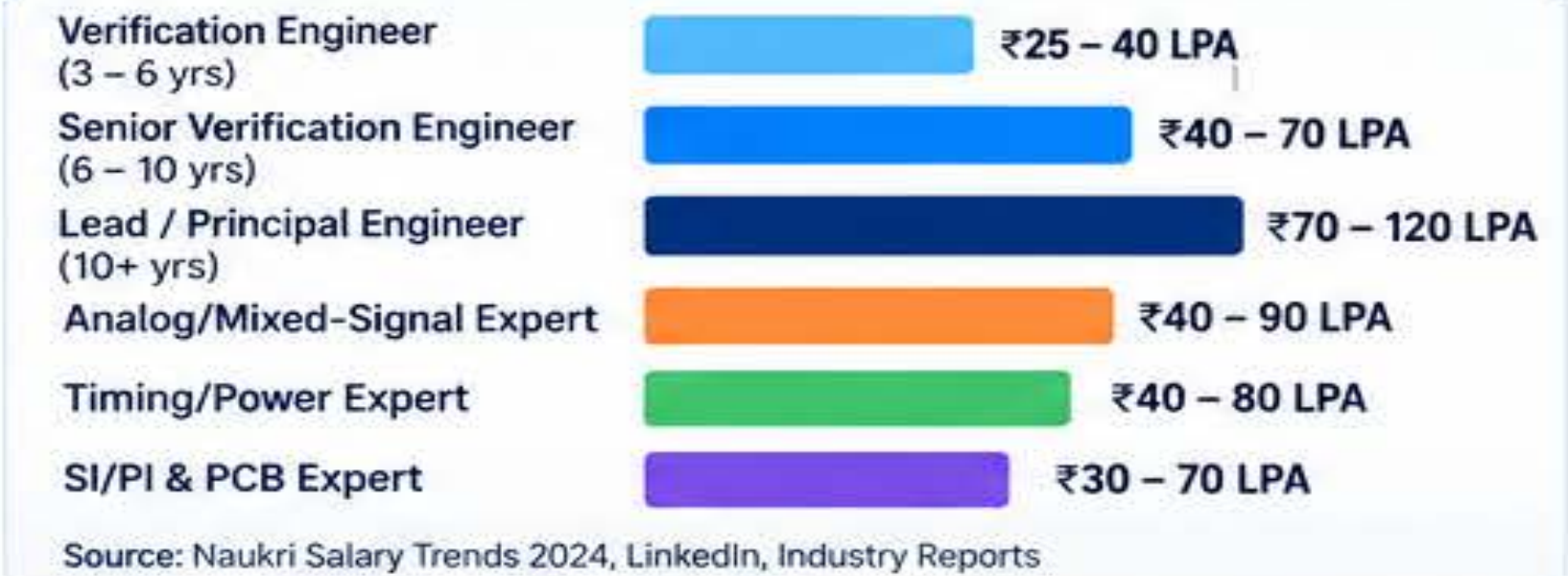
## CHALLENGES FOR ENGINEERING TEAMS

- Multi-domain Expertise Required**  
Need deep knowledge across digital, analog, timing, power, SI/PI, PCB and manufacturing.
- Limited Availability**  
Experts are concentrated in large global companies and GCCs.
- High Hiring Cost**  
Senior verification engineers command premium salaries (₹40 – 90 LPA in India).
- Long Ramp-up Time**  
New hires take 6 – 18 months to become fully productive.
- High Attrition**  
Competition from global firms and GCCs leads to high attrition and knowledge loss.
- Barrier for MSMEs & Startups**  
Early-stage companies cannot access or afford such specialized talent.

## VERIFICATION EXPERTS ARE A SCARCE RESOURCE



## SALARY BENCHMARK (INDIA, 2024)



## IMPACT ON BUSINESSES



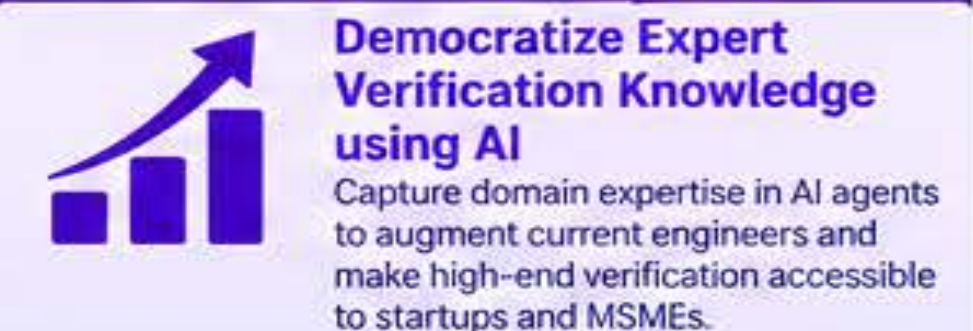
## GLOBAL CONTEXT – TALENT SHORTAGE



## IMPACT ON INDIA'S SEMICONDUCTOR ECOSYSTEM



## THE OPPORTUNITY



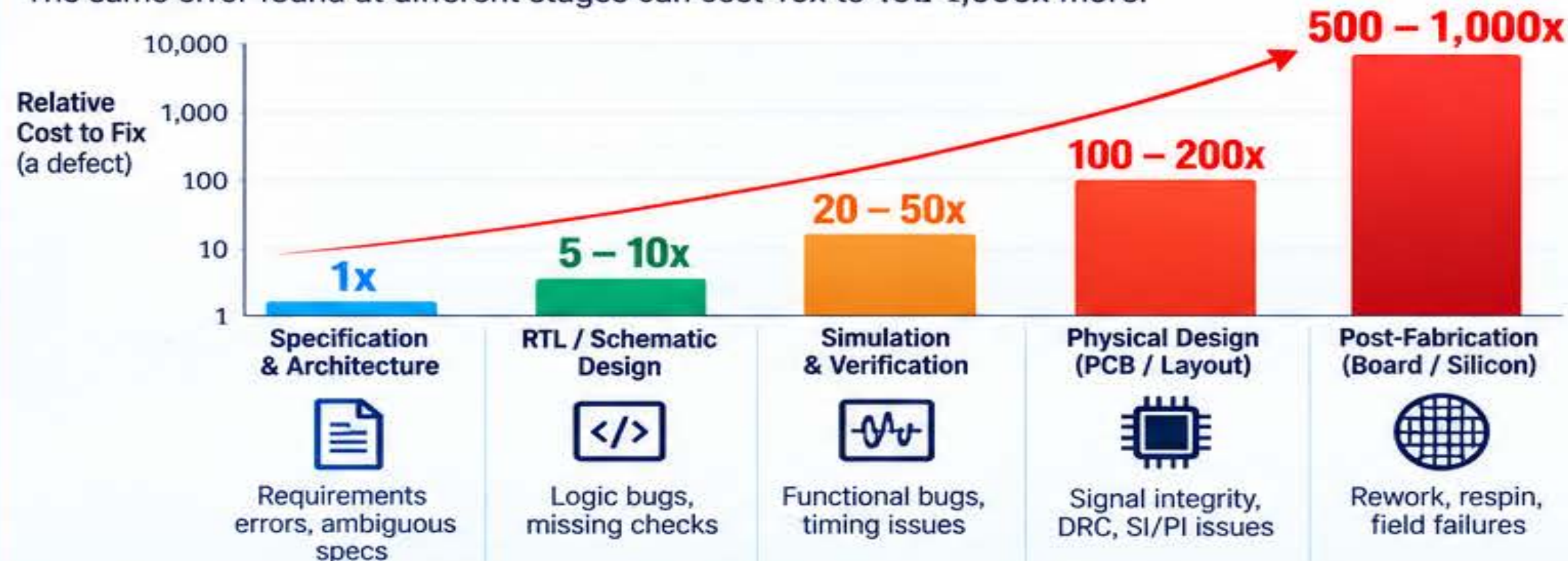
# PROBLEM 4: DESIGN ERRORS BECOME EXTREMELY EXPENSIVE

The later a defect is found, the higher the cost, risk and schedule impact.

**A small design mistake can cost millions and months of delay.**

## COST TO FIX A DEFECT INCREASES DRAMATICALLY

The same error found at different stages can cost 10x to 10e 1,000x more.



## REAL-WORLD COSTS

### PCB / BOARD REWORK



**\$50K – \$500K**

per design issue

- Layout errors, SI/PI problems,
- manufacturing rule violations

**2 – 8 weeks**  
delay for redesign, rework and re-test

### SILICON RESPIN



**\$5M – \$50M+**

per respin

- Logic/timing bugs, power issues,
- analog/mixed-signal errors,
- DFM violations

**6 – 12 months**  
delay (or more) for new silicon, validation and production ramp

## ADDITIONAL IMPACTS



**TIME TO MARKET DELAY**  
**6 – 12 months or more**

loss of market window and revenue opportunity



**REVENUE LOSS**  
**\$10M – \$100M+**  
missed revenue for a delayed product (depending on market)



**REPUTATION RISK**  
Can impact customer trust and future business opportunities, especially in automotive, industrial and consumer electronics

## EXAMPLES FROM INDUSTRY

### CHIP RESPIN – INDUSTRY EXAMPLE



**~\$10M+**

cost for a single advanced-node respin (e.g., 28nm–3nm)

**6 – 12 months**  
delay

(Multiple industry reports: IBS, 2023; SemiEngineering)

### PCB REWORK – REAL CASE



**\$100K – \$500K**

rework cost due to signal integrity / DRC issues on complex boards

**4 – 8 weeks**  
delay

(Industry case studies and engineering consultancies)

### FIELD FAILURE – LARGE SCALE



**\$50M – \$500M+**

recall cost in automotive or consumer products due to hardware defects



Brand and reputation impact for years (Industry analysis)

### CUMULATIVE IMPACT ON PROGRAM



A late-stage defect can increase total development cost by **2 – 5x** and extend schedule by **6 – 18 months**.

(McKinsey, Synopsys, Cadence, industry reports)

## WHY ERRORS ESCAPE EARLY?



**Ambiguous Requirements**  
Incomplete or unclear specs



**Incomplete Verification**  
Missing corner cases and checks



**Tool & Flow Complexity**  
Multiple tools, disconnected flows



**Human Limitations**  
Hard to catch all issues manually

## BUSINESS IMPACT SUMMARY



**2 – 5x**  
higher total development cost



**6 – 18 months**  
schedule delay



**\$10M – \$100M+**  
potential revenue loss



**Higher risk**  
of field failures, recalls and brand damage

## THE OPPORTUNITY WITH PRAGYAN AI



Catch errors **early** with AI-powered verification agents



Automatic constraint checks, DRC, SI/PI and protocol analysis



Reduce rework, respin risk and development cost



Faster, more reliable path from design to silicon / production



# PROBLEM 5: LONG VERIFICATION CYCLES DELAYS TIME-TO-MARKET

Manual, iterative verification takes months to years, slowing product launches and market opportunities.



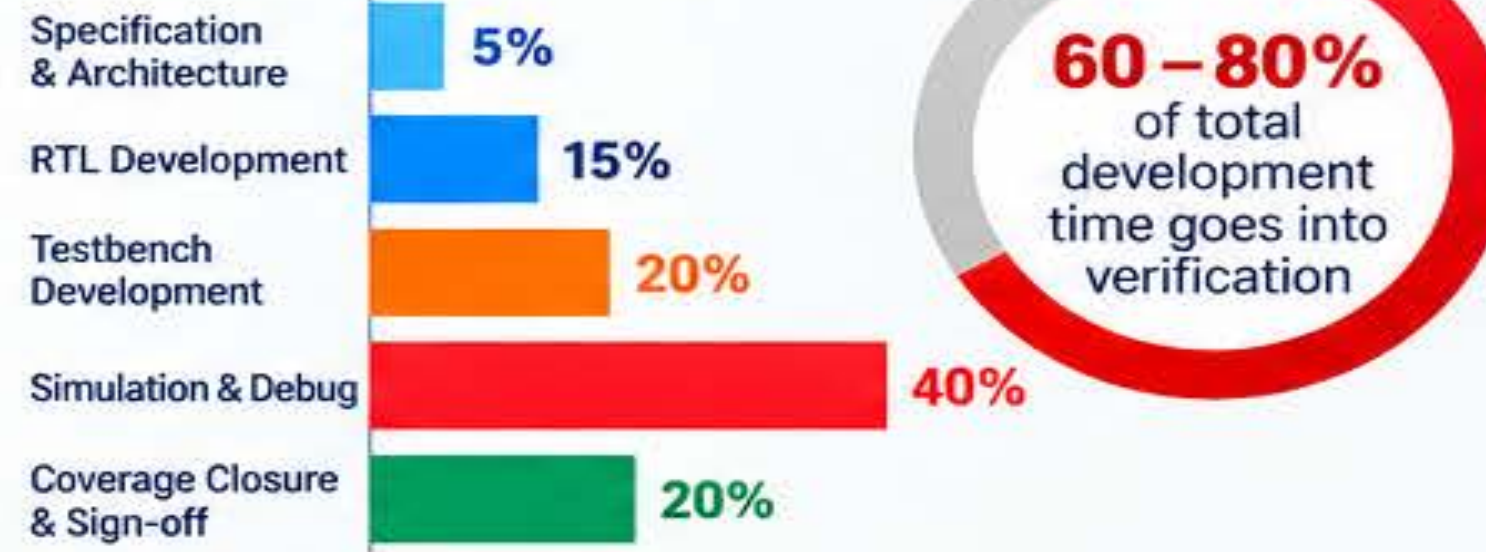
**Time lost today means revenue lost tomorrow.**

## TRADITIONAL VERIFICATION FLOW – SLOW & ITERATIVE



## VERIFICATION TIME IN REAL DESIGNS

**Average time spent in verification**  
(% of total design cycle)



**TYPICAL VERIFICATION TIMELINE**  
(Complex SoC / ASIC)



Source: Mentor/Siemens EDA, Synopsys, McKinsey, Industry Interviews (2023–24)

## BUSINESS IMPACT



**6 – 18 months**

average delay in time-to-market due to verification cycles

Late entry loses market share



**\$10M – \$100M+**

revenue at risk for a delayed product (depends on market)

Competitors capture opportunity



**2 – 5x**

higher total development cost due to extended schedules

Higher engineering burn rate



**Increased risk**

of last-minute bugs, silicon respins and customer dissatisfaction

Brand and reputation impact

## MARKET FACTS & DATA



**50+**

fabless semiconductor companies in India targeting next DLI phase

Faster time-to-market is critical



**\$70B+**

global semiconductor market for AI, automotive, HPC by 2030 (CAGR ~12%)

High competition rewards first movers



**35%**

of projects miss their original tape-out schedule due to verification issues

Schedule slips are common and costly

Source: McKinsey Semiconductor Report (2023), SEMI (2024), Industry Surveys

## TRADITIONAL APPROACH

**18 – 36 MONTHS** (Complex SoC)



Manual process and iterations



60 – 80% time in verification



High compute infrastructure cost



Schedule slips common

**VS**

## PRAGYAN AI – AI-POWERED VERIFICATION

**4 – 12 MONTHS** (Equivalent Design)



AI agents automate test generation



3 – 5x faster verification



Reduced compute cost (20 – 50%)



On-time tape-out



INTELLIGENT AGENTS  
AT EVERY STAGE



REDUCE VERIFICATION TIME  
FROM MONTHS TO WEEKS



LOWER COST.  
FASTER TIME-TO-MARKET.



TURN COMPLEX DESIGNS  
INTO REAL PRODUCTS.



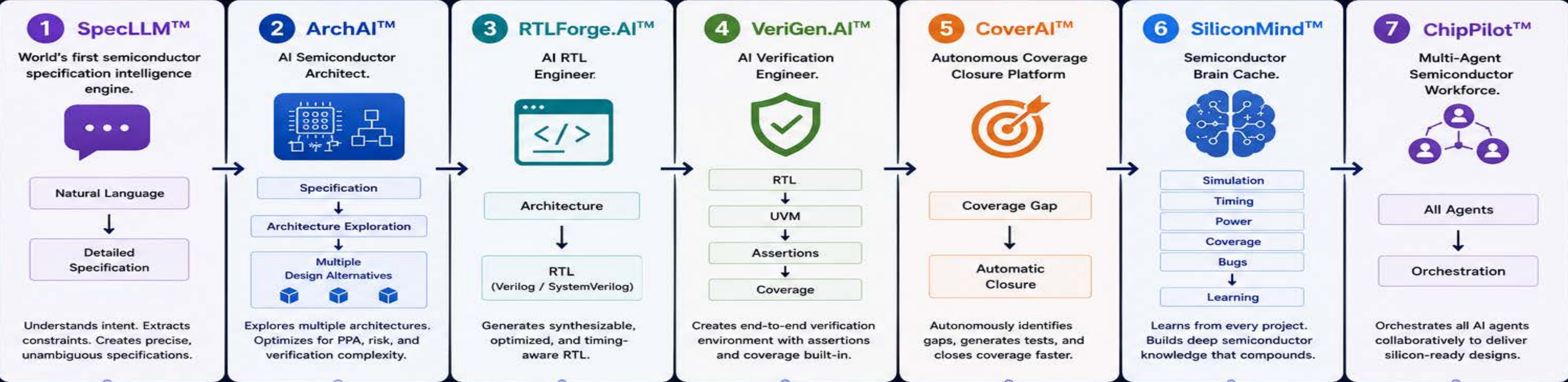
# **Solution & Technology**



# Product/ Solution - Innovation

## PRAGYANAI™ PRODUCT PORTFOLIO

An Autonomous Semiconductor Engineering Workforce – From Natural Language to Silicon



### OUR MOAT – HARD TO COPY, IMPOSSIBLE TO REPLICATE



#### Deep Semiconductor Knowledge Graph

Proprietary graph of protocols, architectures, IPs, RTL patterns, bugs, and silicon learnings.



#### Proprietary Multi-Agent Orchestration

Specialized agents with domain expertise + coordination layer delivering 10X autonomy.



#### Continuous Learning Flywheel

Every project improves the platform. Compounding advantage over time.



#### Human-in-the-Loop Intelligence

Engineers guide, validate and approve. Ensures trust, safety and adoption.



#### Proprietary Datasets & IP Library

Built from real-world designs, verification environments, bugs, and silicon outcomes.



#### Hardware-Aware LLMs & Fine-Tuning

Our LLMs understand timing, power, area, protocols and silicon constraints.



#### Architecture Exploration Engine

Evaluates thousands of architectural choices across PPA, risk, and verification metrics.



#### End-to-End Platform Moat

From spec to silicon with feedback loops. Point solutions can't compete.

### OUR NOVELTY – WHAT'S NEW & DIFFERENT



**SpecLLM™ – First Semiconductor Specification Intelligence Engine**  
Understands natural language intent and generates detailed, industry-grade specifications automatically.



**Multi-Agent Semiconductor Workforce**  
Not a single LLM, but a team of fine-tuned domain agents working together like an expert engineering organization.



**Autonomous Coverage Closure (CoverAI™)**  
First platform to autonomously close coverage with minimal human effort.



**SiliconMind™ – The Semiconductor Brain Cache**  
A persistent memory of every project, decision, bug, and learning.



**Human-in-the-Loop Architecture**  
Combines AI speed with human judgment for safety-critical correctness.



**End-to-End Autonomous Engineering**  
Only platform that connects requirements → architecture → RTL → verification → closure → silicon with continuous feedback.



### COMPETITIVE ADVANTAGE SUMMARY



**10X**  
Faster Design Cycle



**80%+**  
Bug Reduction



**70%+**  
Verification Effort Reduction



**40%+**  
Lower Engineering Cost



Higher Quality First-Pass Silicon Success

#### OUTCOME

#### SILICON READY

Smarter. Faster. Autonomous.  
From Natural Language to Silicon.



# Product/ Solution - Innovation



## RTL Design & Verification from Specification

### AI-Driven End-to-End Autonomous Workflow



From Natural Language  
Spec to Verified RTL



Multi-Agent AI  
Co-Engineering



Faster Development  
Lower Re-spins



Production-Ready  
Design & Verification

#### 1 Specification (Natural Language / Document)

Example Spec:  
Design a 32-bit AXI4  
LED controller with  
memory-mapped  
registers, PWM control,  
interrupt support and  
test mode.  
  
Provide high-level  
requirements, interfaces,  
timing and constraints.



Requirements Documents  
/ Natural Language

#### 2 AI Spec Analysis & Refinement



Understand requirements  
and extract functionality



Generate architecture  
and micro-architecture



Define interfaces  
(AXI, APB, etc.)



Identify corner cases  
and verification plan

#### 3 RTL Design Generation

```
led_controller.v
module led_controller (
    input logic clk,
    input logic rst_n,
    input logic [31:0] axi,
    ...
    // AXI interface
    // LED control logic
    // Registers
    // PWM generation
    // Interrupt logic
endmodule
```



AI-Generated  
Clean & Synthesizable RTL

#### 4 Verification Environment Generation

```
tb_led_controller.sv
class axi_driver;
// AXI driver
endclass

class axi_monitor;
// AXI monitor
endclass

class led_scoreboard;
// Scoreboard
endclass

// UVM Testbench
module tb_led_controller;
// UVM environment
endmodule
```



AI-Generated  
UVM Testbench, Assertions  
and Test Cases

#### 5 Simulation, Analysis & Debugging

##### Simulation Waveforms



##### Assertion & Coverage

- ✓ Assertions: 124 / 124 Passed
- ✓ Functional Coverage: 92%
- ✓ Code Coverage: 89%



##### AI-Powered Debugging

- ! Root cause analysis and  
fix suggestions for failures

#### 6 Verified RTL (Ready for Synthesis)



- ✓ Functionally Correct
- ✓ Assertions Passed
- ✓ High Coverage
- ✓ Clean & Synthesizable
- ✓ Ready for Integration

### Multi-Agent AI Co-Engineering



**Spec Agent**  
Understands and refines  
requirements



**Architect Agent**  
Creates system and micro-  
architecture



**Coder Agent**  
Generates RTL and supporting  
modules



**Verification Agent**  
Creates UVM, Assertions and  
Test Scenarios



**Debug Agent**  
Analyzes failures and suggests  
fixes



**Optimizer Agent**  
Improves timing, area and power

#### Supports Multiple Standards

AXI / AXI4

AHB / APB

RISC-V

Custom IP

SoC Subsystems

High-Speed Interfaces

### KEY BENEFITS



10x Faster  
RTL Development



Higher  
Verification Coverage



Lower  
Re-spin Cost



Reduces Dependency  
on Expert Engineers



Production-Ready  
Designs



Accelerates  
Time-to-Market



## GENERIC LLM OUTPUT

Looks like Verilog. Fails in Silicon.



**General LLM**  
Trained on internet data  
(Not hardware aware)

### LLM GENERATED VERILOG CODE (Example)

```
always @(posedge clk) begin
    if (enable) begin
        for (i = 0; i < 1024; i = i + 1) begin
            data_out = data_in + 1;
        end
    end
    if (rst) begin
        q = 0;
    end else if (enable) begin
        q = d;
    end
end
```



### SYNTHESIS FAILED

Multiple Errors Found

#### ERRORS (Example)

- ✗ Illegal Clock Gating Detected
- ✗ Implicit Latches Inferred
- ✗ Infinite Loops / Unbounded Iterations
- ✗ Timing Violations
- ✗ Non-synthesizable Constructs
- ✗ Unsupported System Tasks
- ✗ Coding Style Issues

#### SYNTHESIS REPORT (Excerpt)

**Error:** Latch inferred for signal 'q'

**Error:** Un-synthesizable loop in line 3

**Error:** Gated clock detected

**Error:** Timing constraint violation

**Error:** Unsupported constructs

**SYNTHESIS FAILED**



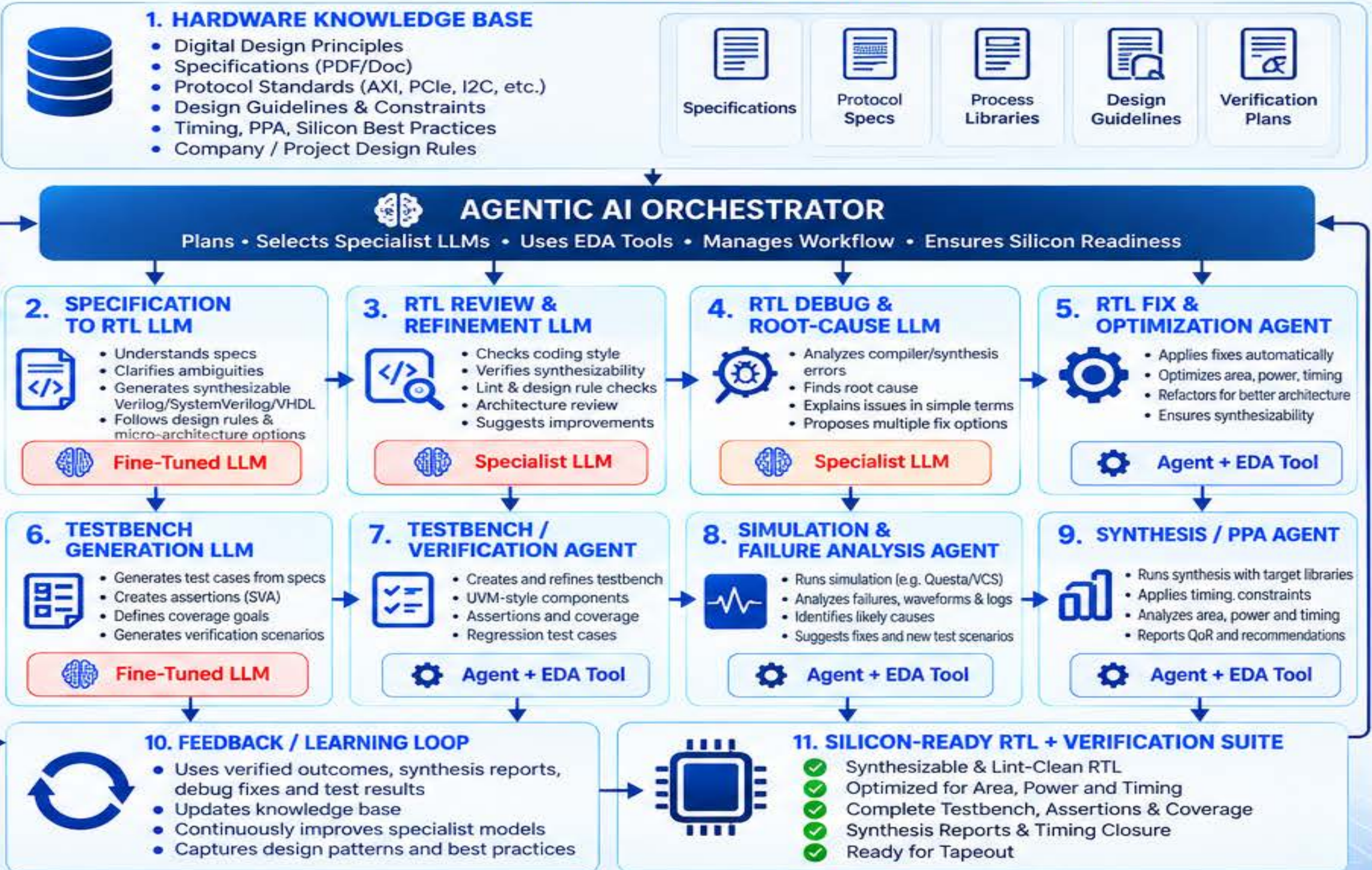
#### WHY IT HAPPENS

- General LLM lacks hardware design understanding
- May generate syntactically correct but non-synthesizable RTL
- Not aware of design rules, timing, PPA
- No awareness of target libraries or constraints
- Trained on public data, not silicon-proven designs

VS

## PRAGYAN AI HARDWARE-AWARE AI

Multi-Specialist LLMs + EDA Tools + Engineering Intelligence  
**Understands Hardware. Delivers Silicon-Ready RTL.**



NOT JUST CODE GENERATION.  
ENGINEERING INTELLIGENCE.



MULTI-SPECIALIST LLMs  
FOR EACH ENGINEERING TASK.



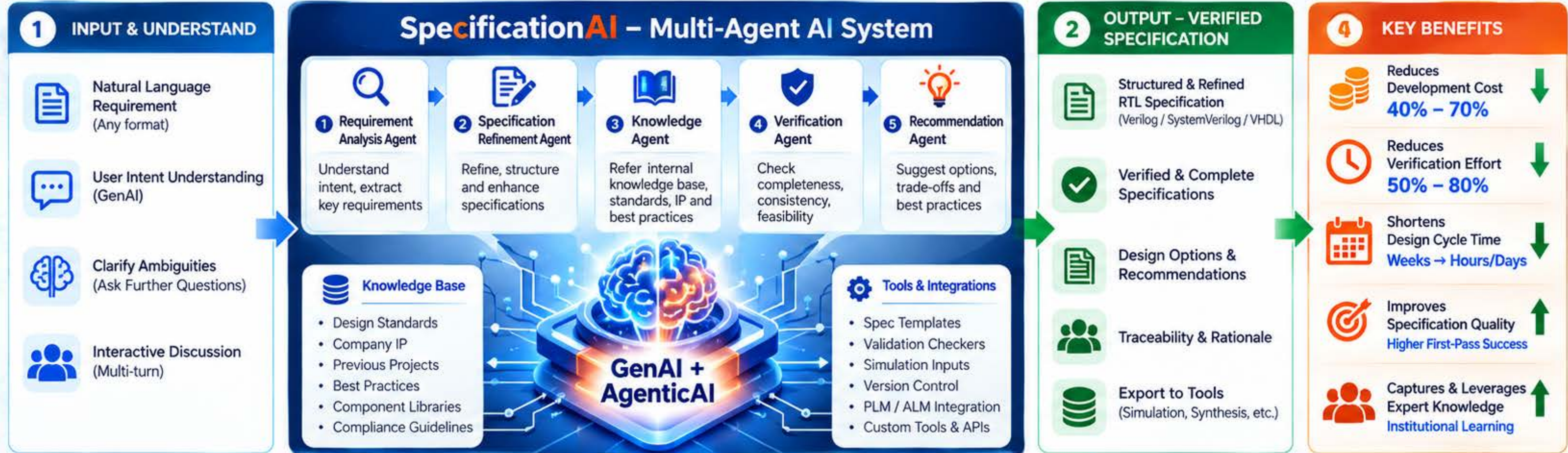
INTEGRATED WITH  
INDUSTRY EDA TOOLS.

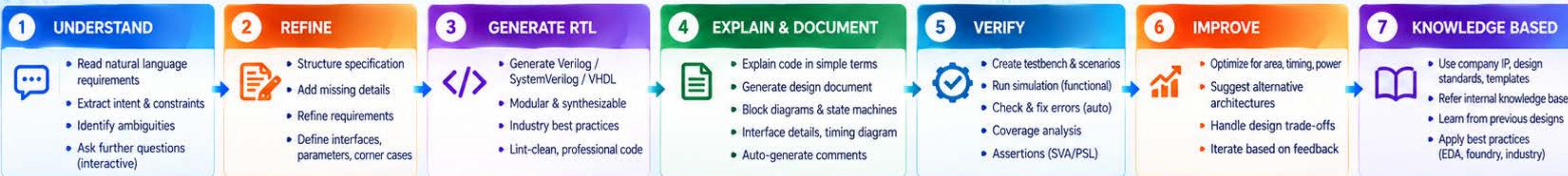


DELIVERS SILICON-READY RTL  
WITH VERIFICATION SUITE.

GenAI and AgenticAI for Smarter, Faster, and Higher Quality Hardware Specifications

INTELLIGENCE | COLLABORATION | AUTOMATION | VERIFICATION | KNOWLEDGE DRIVEN







## 1 INPUT



## 2 AI ANALYSIS AGENTS



- Code Analysis Agent
- Log Analysis Agent
- Waveform Analysis Agent
- Root Cause Agent
- Spec Traceability Agent
- Fix & Refinement Agent

## 3 ROOT CAUSE & INSIGHTS



- Identify Failure & Symptom
- Analyze Signal Behavior
- Trace to RTL Code
- Map to Specification
- Determine Root Cause
- Highlight Similar Past Issues (Knowledge Graph)

## 4 SUGGEST FIX & REFINEMENT



- Provide Code Fix
- Explain the Fix
- Check for Side Effects
- Suggest RTL Refactoring
- Generate Regression Tests
- Validate with Simulation

## 5 VERIFIED OUTPUT



- Fixed RTL Code
- Updated Test Case
- Validation Results
- Coverage Improvement
- Documentation & Notes

## 1 FAILURE INPUT

### RTL Code (Buggy)

```
counter.sv
1 module counter (
2   input clk,
3   input rst_n,
4   input en,
5   output reg [7:0] count
6 );
7   always @(posedge clk) begin
8     if (!rst_n)
9       count <= 8'd0;
10    else if (en)
11      count <= count + 1;
12  end
13 endmodule
```

### Simulation Error Log

```
# ** Error: counter_tb.sv(45);
# Assertion failed: count should
# not increment when en=0
# Time: 250 ns
# ** Fatal: Simulation stopped.
```

### Waveform (VCD/FSDB)



### Assertion (SVA)

```
1 property p_no_increment;
2   @(posedge clk)
3     disable if (!rst_n)
4     !en |-> $stable(count);
5 endproperty
6
```

### Test Case

```
// en should be 0, count must remain stable
en = 0;
repeat (5) @(posedge clk);
if (count != prev_count) $error("Count changed");
```

## 2 AI ANALYSIS & ROOT CAUSE

- Code Analysis**  
Checks RTL for coding errors, synthesizability issues, latches, race conditions and bad practices.
- Waveform Analysis**  
Analyzes signal transitions, finds first divergence and correlates with failure time.
- Spec Traceability**  
Maps RTL behavior to the specification requirement.
- Root Cause: Identification**  
**Root Cause:** Counter increment condition is incorrect. The enable condition is not properly handled due to missing else branch or incorrect logic, causing count to increment even when en = 0.

- Related Issues (Knowledge Graph)**
- Similar issue found in previous project
  - Common in counter/enable logic
  - Recommended design pattern available

## 3 AI SUGGESTED FIX & REFINEMENT

### Fixed RTL Code

counter\_fixed.sv

```
1 module counter (
2   input clk,
3   input rst_n,
4   input en,
5   output reg [7:0] count
6 );
7   always @(posedge clk) begin
8     if (!rst_n)
9       count <= 8'd0;
10    else if (en)
11      count <= count + 1;
12    else
13      count <= count; // Hold value
14  end
15 endmodule
```

### Explanation

- Added else branch to hold count when en = 0
- Prevents unintended increment
- Aligns with specification requirement
- Synthesizable and safe for FPGA/ASIC



### Additional Refinements (AI Suggestions)

- Use parameterizable width
- Add reset synchronization (if needed)
- Add assertions for overflow conditions
- Consider using always\_ff for better style
- Add coverage points

## 4 VALIDATION & RESULTS

- ✓ Compilation Successful
- ✓ All Assertions Passed
- ✓ Test Case Passed
- ✓ Waveform Verified
- ✓ Coverage Improved

### Waveform (Fixed)



### Regression Test (Auto-Generated)

```
1 // Test to verify counter behavior
2 task test_no_increment();
3   en = 0;
4   repeat (10) @(posedge clk);
5   assert(count == prev_count);
6 endtask
```

## KEY BENEFITS



Faster  
Root Cause  
Analysis



Reduced  
Debug Time  
40% - 70%



Higher  
RTL Quality



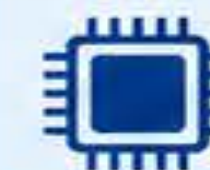
Specification  
Compliance



Reuse Learning  
Across Projects  
(Knowledge Graph)



Better  
Verification  
Coverage



**CLEAN RTL.  
FASTER DEBUG.  
HIGHER QUALITY SILICON.**

### 1 SPEC TO RTL

Turn Requirements into High-Quality RTL



Natural Language / Specification  
"Design a 32-bit RISC-V core with AXI interface, 4-stage pipeline, low power mode..."



Requirement Analysis



Architecture Understanding



RTL Generation



Code Review & Lint



Refinement

#### Generated RTL (SystemVerilog)

```
module riscv_core (  
  input logic clk,  
  input logic rst_n,  
  ...  
);  
  // Generated RTL  
endmodule
```

- ✓ Requirement to RTL in minutes
- ✓ Supports multiple standards
- ✓ Context-aware code generation

### 2 TESTBENCH & VERIFICATION

Auto-Generate Complete Verification Environment



Specification + RTL



UVM Testbench Generation



Test Case Generation



Assertions (SVA)



Protocol Verification



Environment Setup

#### UVM Testbench Architecture



- ✓ Functional, boundary, negative tests
- ✓ UVM environment auto-generated
- ✓ Protocol & interface validation

### 3 SIMULATION & ANALYSIS

Run, Analyze and Find Issues Automatically



Compile



Simulate



Analyze

#### Simulation Results

```
# UVM_INFO @ 1300ns : test_passed  
# UVM_INFO @ 1450ns : coverage update  
# ERROR : assertion failed at top.sv:102  
# Waveform dump generated  
# Analysis completed
```

#### AI Analysis

- 🏠 Detects failures & errors
- 🔍 Finds root cause
- 👤 Analyzes waveforms
- 🗨 Explains with context
- 🛠 Suggests fixes

#### Waveform Analysis



- ✓ Automated log & waveform analysis
- ✓ Root-cause identification
- ✓ Natural language explanations

### 4 CODE COVERAGE

Achieve Maximum Coverage with AI

#### Coverage Analysis

|           |     |
|-----------|-----|
| Statement | 98% |
| Branch    | 92% |
| Toggle    | 88% |
| FSM       | 85% |
| Path      | 78% |

#### Coverage Gaps

- 🔴 Uncovered branch at state IDLE
- 🔴 Missing corner case for max value
- 🔴 Unreachable state in FSM

#### AI-Powered Closure

- 📄 Generate targeted tests
- 🔧 Suggest RTL changes (if needed)
- 🔄 Re-run simulation
- 📊 Track progress

#### Coverage Report



- ✓ Finds uncovered scenarios
- ✓ Generates tests for closure
- ✓ Tracks coverage progress

### 5 ANALYZE & IMPROVE

Get Insights, Optimize Design, Reduce Risks



#### AI Analysis

- 📄 Code Quality & Best Practices
- 📈 Performance & PPA Impact
- 🔒 Security & Compliance
- ⚠ Design Risks & CDC/Reset
- ⚙ Change Impact Analysis



#### Suggested Improvements

- 💡 Refactor complex logic
- 💡 Optimize critical paths
- 💡 Fix risky constructs
- 🕒 Improve test coverage
- 📄 Update documentation

#### Before → After

| Before        | After         |
|---------------|---------------|
| CPI: 1.32     | CPI: 1.12     |
| Area: 1.8 mm² | Area: 1.6 mm² |
| Power: 420 mW | Power: 360 mW |

- ✓ Actionable insights
- ✓ Performance & power gains
- ✓ Reduced risk and rework

### 6 VERIFICATION SUCCESS

Confidence in Every Build

- ✓ All tests passed
- ✓ Coverage closure > 95%
- ✓ No critical warnings
- ✓ Formal checks passed
- ✓ Security checks passed
- ✓ Signoff ready



#### Build Report

- 📄 Test Summary
- 📄 Coverage Report
- 📄 Lint & CDC Report
- 📄 Formal Report
- 📄 Security Report
- 📄 Recommendation List

- ✓ Signoff-ready reports
- ✓ Traceable results
- ✓ Full transparency



Powered by  
**PRAGYAN AI**

#### AI AGENTS



Spec Agent  
(Understand)



Code Agent  
(Generate)



Verify Agent  
(Test & Simulate)



Debug Agent  
(Analyze & Fix)



Coverage Agent  
(Closure)



Refine Agent  
(Optimize)

#### KEY BENEFITS



Faster  
Time-to-Market



Higher  
Quality



Lower  
Rework Cost



Smarter  
Engineering

Home

AI Tutor

Learning Path

Hands-on Labs

Projects

Quizzes & Assessment

My Progress

Bookmarks

Community

Resources

Settings

Ask anything.  
Learn by doing.  
Build with confidence.

Start Learning with AI Tutor

Specification

Architecture

RTL Design

Testbench

Simulation

Coverage

Debug

Signoff

SpecificationAI Tutor

Architecture Tutor

RTL Code Generation Tutor

Test Bench Tutor

Simulation Tutor

Coverage Tutor

Debug Tutor

Verification Tutor

SpecificationAI Tutor

I want to design a PCIe Gen5 x4 controller. Can you help me refine the specification? What are the key requirements I should consider?

Great! Let's refine the specification. Here are the key areas and some questions:

- Functional Requirements**
  - Gen5 x4 (16 GT/s per lane) – is this correct?
  - Endpoints: Root Port or End Point or Both?
  - Supported features: Enumerations, MSI/MSI-X?
- Interface & Protocol**
  - Transaction layer (TLP) support?
  - Flow control, ordering, completion handling?
- Performance**
  - Target throughput, latency requirements?
- Power & Area**
  - Low power modes (L0s, L1, L2)?
  - Power budget and process node?
- Environment**
  - Target platform (SoC, FPGA, ASIC)?
  - Verification environment (UVM)?

**Missing Information / Clarifications**

- Do you need multi-function support?
- Any specific memory or I/O requirements?
- What are the compliance / certification targets?
- Are there any custom features or extensions?

Refine Specification

Generate PRD

Create Requirement Matrix

Ask your question here...

Interactive Learning Lab

Examples

Try it Yourself

AI Feedback

Quizzes

Notes

1 Specification to RTL

Natural Language / Spec

"4-bit counter with synchronous reset and enable"

AI Analysis & Refinement

- Extract functional requirements
- Identify interfaces (clk, rst, en, count)
- Check for missing details
- Suggest improvements

Generated RTL (Verilog)

```

module counter #(parameter WIDTH=4)(
    input wire clk,
    input wire rst_n,
    input wire en,
    output reg [WIDTH-1:0] count
);
    always @(posedge clk) begin
        if (rst_n)
            count <= 0;
        else if (en)
            count <= count + 1;
        # 10ns
    end
endmodule
                    
```

Generate Testbench

Add Assertions

2 Test Bench Tutor

- Generate UVM/SV testbench
- Create test scenarios
- Add assertions and coverage
- Explain each component

Testbench (SV/UVM)

```

class counter_test extends uvm_test;
    counter_env env;
    function void build_phase(...);
        env = counter_env::type_id::create(
            "env", this);
    endfunction
    task run_phase(...);
        repeat(100) begin
            env.drv.randomize();
            env.drv.drive();
        end
    endtask
endclass
                    
```

Assertions (SVA)

```

property p_count_increment;
    @(posedge clk) disable iff (rst_n)
    en ==> (count == $past(count)+1);
endproperty
                    
```

Generate Waveform

Explain Code

3 Simulation & Analysis

- Run simulation (EDA tool integration)
- Analyze waveforms and logs
- Identify mismatches
- Explain results in simple terms

Waveform Viewer

Simulation Log (Console)

```

# ** Info: Simulation started
# ** Info: Test counter_test started
# ** Info: 100 cycles completed
# ** Info: No errors detected
# ** Info: Simulation finished
                    
```

Run Simulation

Analyze Waveform

Explain Results

4 Coverage Tutor

- Functional, Code and Assertion Coverage
- Identify missing scenarios
- Suggest additional tests
- Auto-generate tests for coverage closure

Coverage Report

82%

76%

90%

Functional

Code

Assertion

Uncovered Scenarios

| ID | Description               | Type       |
|----|---------------------------|------------|
| 1  | Reset during enable       | Functional |
| 2  | Counter wrap-around       | Functional |
| 3  | Enable toggle at clk edge | Assertion  |
| 4  | Illegal state transition  | Code       |

Show Coverage Details

Suggest Tests

Generate Tests for Gaps

5 Debug Tutor

- Analyze errors and failures
- Find root cause with AI
- Suggest fixes and code changes
- Explain why the bug occurred

Root Cause

Enable signal is not gating the increment in this condition.

Suggested Fix

```

if (en)
    count <= count + 1;
                    
```

6 Architecture Tutor

- Explore architecture options
- Compare performance, area, power
- Analyze trade-offs with AI
- Generate block diagrams

7 Verification Tutor

- Verification plan and strategy
- Test planning and coverage model
- Generate assertions and checks
- Compliance and signoff guidance

Verification Plan

Coverage Model

Compliance Checklist

Signoff Readiness

8 Learning & Practice

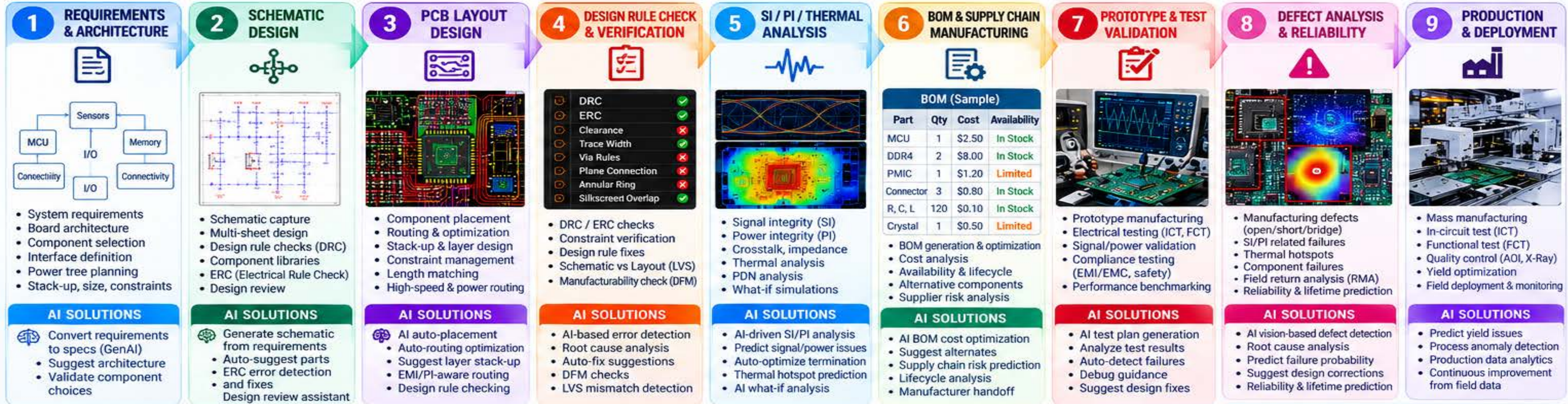
- Step-by-step explanations
- Hands-on exercises
- Quizzes and assessments
- Real industry use cases

Interactive Examples

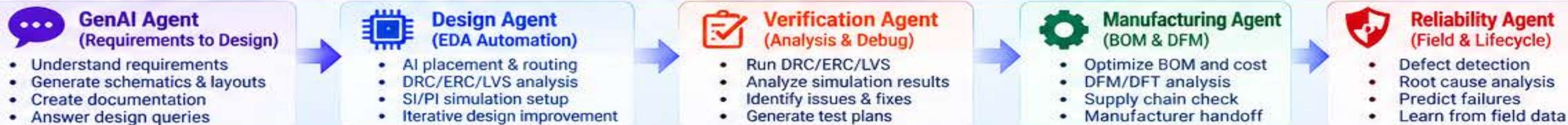
Hands-on Labs

Quizzes

Projects



## PRAGYAN AI MULTI-AGENT AI OS FOR BOARD ENGINEERING



## EDA TOOL ECOSYSTEM (Works with Your Existing Tools)

Altium cadence SIEMENS KEYSIGHT ZUKEN ...

## EXAMPLE RESULTS (INDUSTRY USE CASES)



## KEY BENEFITS WITH PRAGYAN AI



# PCB AI COPILOT

## Design Safer PCBs. Faster. Smarter.

AI-powered design review, verification and manufacturing intelligence for high-quality, cost-effective and reliable PCBs.

- ✓ DFM Checks
- ✓ EMI/EMC Analysis
- ✓ Thermal Intelligence
- ✓ Defect Prediction
- ✓ Design Optimization

### 1 Input Design Files

Upload PCB design files and requirements.



Schematic, Layout, Gerber, BOM, Mechanical Files

### 2 AI Design Analysis

AI agents analyze design for electrical, manufacturing and reliability issues.

- 🔍 Rule & DFM Check
- 📶 EMI/EMC Analysis
- 🔥 Thermal Analysis
- 🔧 Component Validation
- ⚠️ Design Rule Violations

### 3 AI Insights & Issues

Detect issues with root cause analysis and AI suggestions.



- ⚠️ Clearance Violations
- ⚠️ EMI Risk Areas
- ⚠️ Thermal Hot Spots
- ⚠️ Impedance Mismatch
- ⚠️ Component Placement Issues
- ⚠️ Manufacturing Risks

### 4 AI Recommendations

Get actionable suggestions to fix and optimize.

- 🔧 Auto-fix Suggestions
- 🔄 Optimized Routing
- 📍 Better Component Placement
- 🔥 Thermal Improvements
- 🛡️ EMI Mitigation Techniques
- ⚙️ DFM Optimization
- 📋 Standards Compliance (IPC, JEDEC, etc.)

### 5 Optimized PCB

Generate improved design with verified results.



- ✓ Reduced EMI
- ✓ Better Thermal Performance
- ✓ Manufacturing Ready
- ✓ Higher Reliability

### KEY BENEFITS

- 🚀 **Faster Design Cycle**  
Reduce review time by 70%+
- 🛡️ **Lower Re-spin Cost**  
Detect issues early
- 🔧 **High-Quality & Reliable PCBs**  
Fewer field failures
- ₹ **Manufacturing Ready**  
Optimized for DFM/DFT
- 📋 **Standards Compliance**  
IPC, JEDEC, EMI/EMC guidelines
- 🌿 **Cost & Performance Optimized**  
Better component and layout choices

### AI CAPABILITIES

- DFM Checks**  
Manufacturing rule validation
- EMI/EMC Intelligence**  
Identify EMI risk and signal integrity issues
- Thermal Analysis**  
Detect hot spots and optimize cooling design
- Gerber Analysis**  
Review fabrication files and detect manufacturing risks
- Component Intelligence**  
Validate components and suggest alternatives
- AI Auto-Correction**  
Suggest and apply layout improvements

### SUPPORTED FILE FORMATS

- Altium
- KiCad
- EAGLE
- OrCAD
- GERBER
- BOM (CSV/XML)
- STEP
- PDF

### PRIMARY CUSTOMERS

- Electronics MSMEs
- Hardware Startups
- PCB Designers
- Automotive Electronics
- Industrial Electronics
- Medical Devices
- Consumer Electronics

# Core IP II: PCB Review Copilot (Predictive Generative Design)



PCB SENTINEL AUTONOMOUS INSPECTION SYSTEM

AGENTS ONLINE: 3

DEFECTS

|                                                                                                                          |                                                                                                                                                       |
|--------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Corrosion and Solder Mask Failure</b> <b>HIGH</b>                                                                     | <b>Trace Damage / Erosion</b> <b>HIGH</b>                                                                                                             |
| <b>Description:</b><br>Widespread failure of the solder mask ... corrosive agent (e.g., battery acid or liquid ingress). | <b>Description:</b><br>The exposed copper traces show heavy reddish-brown erosion ... discontinuity or severe reduction in current carrying capacity. |
| <b>Location:</b> Central trace bundle to locatus in the 'VCC' and '3V' labels.                                           | <b>Location:</b> Area circled on the right ... traces clustered on the left.                                                                          |

## Technical Specs

**Core Model:** Fine-tuned Vision Transformer (ViT) trained on 1,000+ proprietary defect images.

**Capability:** Real-time inference (<5 seconds) to identify EMI hotspots, 90-degree acid traps, and high-impedance discontinuities.

**The Moat:** Moves verification from slow post-layout simulation to instant physics-aware spell-checking during the layout phase. Reduces fabrication re-spins by 60%.

### 1 REQUIREMENTS & ARCHITECTURE TUTOR

System to Board Planning

- Explain concepts
- Analyze requirements
- Suggest architecture
- Check feasibility & cost
- Ask/answer questions
- Exercises & quizzes

### 2 SCHEMATIC DESIGN TUTOR

Capture & Validate

- Explain design rules
- Review schematic
- Identify issues
- Suggest improvements
- Run ERC checks
- Step-by-step guidance

### 3 PCB LAYOUT DESIGN TUTOR

Placement, Routing, Stackup

- Guide placement & routing
- Optimize stackup
- Check clearances
- Suggest routing strategies
- Maintain SI/PI best practices
- Interactive design exercises

### 4 DRC/ERC & VERIFICATION TUTOR

Design Rule & Constraint Check

- Explain DRC/ERC rules
- Analyze violations
- Suggest fixes
- Check constraints
- Auto-review uploaded design
- Learn from real examples

### 5 SI/PI/THERMAL ANALYSIS TUTOR

Signal, Power & Thermal Integrity

- Run SI/PI/thermal analysis
- Explain results (eye, S-parameters)
- Find issues & hotspots
- Suggest mitigation (termination, decoupling, plane)
- What-if analysis
- Visualize and learn step-by-step

### 6 BOM & SUPPLY CHAIN TUTOR

Parts, Cost & Availability

| Part      | Qty | Cost   | Availability |
|-----------|-----|--------|--------------|
| MCU       | 1   | \$2.50 | In Stock     |
| DDR4      | 2   | \$8.00 | Limited      |
| PMIC      | 1   | \$1.20 | In Stock     |
| Connector | 4   | \$0.80 | In Stock     |
| Crystal   | 1   | \$0.30 | In Stock     |
| Inductor  | 2   | \$0.20 | Limited      |

- Suggest alternate parts
- Check cost and availability
- Compare suppliers
- Lifecycle & risk analysis
- Optimize BOM (cost/performance)
- Generate procurement reports

### 7 PROTOTYPE & TEST TUTOR

Bring-up & Validation

- Guide prototype planning
- Suggest test points
- Explain test procedures
- Analyze lab measurements
- Debug bring-up issues
- Create test checklists

### 8 DEFECT ANALYSIS & RELIABILITY TUTOR

Failure Analysis & Improvement

- Analyze defect images (AI Vision)
- Identify root cause
- Suggest corrective actions
- Reliability & stress analysis
- Learn from real failure cases
- Exercises with examples

### 9 MANUFACTURING & PRODUCTION TUTOR

DFM, DFT & Mass Production

- Check manufacturability (DFM)
- Panelization & yield optimization
- Suggest process settings
- Explain test (ICT, FCT, AOI, X-Ray)
- Review production data
- Guidance for higher yield & quality

## Central AI Tutor

Your interactive guide across the complete PCB/Board lifecycle

- Ask Anything (Text, Image, Files)
- Understand • Explain • Analyze
- Review Your Designs (Schematic, PCB, Reports)
- Identify Issues & Risks
- Generate Suggestions & Alternatives
- Run Simulations & What-if Analysis
- Provide Step-by-Step Guidance
- Create Exercises, Quizzes & Projects
- Personalized Learning Path
- AI Feedback & Progress Tracking

## Multi-Agent AI Engine

Specialized AI Agents Working Together for Accurate, Practical and Reliable Guidance

GenAI Agent  
Understand, Explain, Generate

EDA Tool Agent  
Works with Altium, Cadence, Siemens, etc.

Physics AI Agent  
SI/PI, Thermal, Signal & Power Integrity

Vision AI Agent  
Analyze PCB/Images, Detect Defects

Manufacturing AI Agent  
DFM, DFT, Yield, Supply Chain

Knowledge Graph  
Standards, Best Practices, Real Design Data

### Learning Workspace (Interactive)

AI Tutor Chat

How can I reduce noise on this power rail? Here is my PCB.

I see high impedance in the power loop and insufficient decoupling near the MCU.

Suggested actions:

- Add 100 nF decoupling capacitor near MCU VDD pins
- Shorter and wider power traces
- Use solid ground plane
- Check PDN impedance (run analysis)

Schematic View

PCB Layout View

SI/PI Analysis

Eye Diagram (PCIe)

Power Integrity (PDN)

DRC / ERC Results

| Type         | Description                   |
|--------------|-------------------------------|
| Clearance    | 0.12 mm (min 0.20)            |
| Short        | Net short between GND and VDD |
| Silkscreen   | Overlap with pad              |
| Drill        | Hole size out of range        |
| Width        | Track width < 0.15 mm         |
| Annular Ring | Too small (0.10 mm)           |
| Via          | Unconnected via               |
| Plane        | Split in power plane          |

BOM & Supply Chain

| Part      | Qty | Unit Cost | Status   |
|-----------|-----|-----------|----------|
| MCU       | 1   | \$2.50    | In Stock |
| DDR4      | 2   | \$8.00    | Limited  |
| PMIC      | 1   | \$1.20    | In Stock |
| Connector | 4   | \$0.80    | In Stock |
| Crystal   | 1   | \$0.30    | In Stock |
| Inductor  | 2   | \$0.20    | Limited  |
| Capacitor | 10  | \$0.05    | In Stock |

### Interactive Learning Loop

### Defect Analysis (Vision AI)

Detected: Solder Open  
Confidence: 92%

Likely Cause: Insufficient solder paste or poor reflow profile.

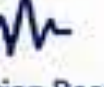
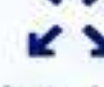
Recommendation: Check stencil, paste volume, and reflow temperature.



### KEY DIFFERENTIATORS / USP

|                                                                                                                                                                                                           |                                                                                                                                                                                                        |                                                                                                                                                                                                                         |                                                                                                                                                                                                                    |                                                                                                                                                                                                                                       |                                                                                                                                                                                                                             |                                                                                                                                                                                                |                                                                                                                                                                                                                                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1</b> <br><b>End-to-End AI Engineering Platform</b><br>Covers System, Chip and Board level in one integrated platform | <b>2</b> <br><b>Domain-Specific AI for Hardware</b><br>Trained on semiconductor, EDA and electronics domain knowledge | <b>3</b> <br><b>Multi-Agent AI Architecture</b><br>Specialized AI agents collaborate for design, verification, PCB and manufacturing | <b>4</b> <br><b>Faster Development &amp; Higher Productivity</b><br>Weeks to days for spec-to-RTL, verification, and PCB design | <b>5</b> <br><b>Higher Quality &amp; Early Defect Detection</b><br>AI-driven analysis, simulation and checks reduce design errors and re-spin risk | <b>6</b> <br><b>Works with Existing EDA Ecosystem</b><br>Integrates with industry EDA tools (Synopsys, Cadence, Siemens, Ansys and more) | <b>7</b> <br><b>Lower Engineering Cost</b><br>Reduces manual effort, expert dependence and iteration cycles | <b>8</b> <br><b>AI Tutors for Learning &amp; Upskilling</b><br>Interactive AI tutors for specification, RTL, verification, PCB, SI/PI and more |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### TECHNOLOGY STACK

|                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                        |                                                                                                                                      |                                                                                                                                             |                                                                                                                                            |                                                                                                                                       |                                                                                                                                                     |                                                                                                                                      |
|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <b>Application Layer</b><br>(AI Engineering Solutions) | <br><b>SpecificAI</b><br>(Specification Intelligence)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | <br><b>SpecTO RTL</b><br>(Automatic RTL Generation)   | <br><b>End-to-End RTL Verification</b>             | <br><b>PCB Design</b><br>(End-to-End)                    | <br><b>BOM Analysis &amp; Optimization</b>              | <br><b>Defect Analysis &amp; Root Cause</b>        | <br><b>AI Tutors</b><br>(Design, Verification, PCB, SI/PI, etc.) |                                                                                                                                      |
| <b>AI Agents Layer</b><br>(Multi-Agent AI OS)          | <br><b>Planner Agent</b><br>(Task planning & orchestration)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | <br><b>Spec Agent</b><br>(Requirement understanding) | <br><b>Design Agent</b><br>(RTL/PCB generation)    | <br><b>Verification Agent</b><br>(Testbench & coverage) | <br><b>Analysis Agent</b><br>(PPA, SI/PI, reliability) | <br><b>Debug Agent</b><br>(Root cause analysis)   | <br><b>Manufacturing Agent</b><br>(DFM, test & yield)           | <br><b>Tutor Agent</b><br>(Interactive learning) |
| <b>Foundation &amp; AI Models</b>                      | <br><b>GenAI</b><br>(LLMs)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | <br><b>Agentic AI</b><br>(Planning & Tool Use)      | <br><b>Physics AI</b><br>(Physics-aware Modeling) | <br><b>Vision AI</b><br>(Layout, Schematic, Defect)    | <br><b>Domain LLM</b><br>(Semiconductor & EDA)        | <br><b>Knowledge Graph</b><br>(Design Knowledge) | <br><b>RAG</b><br>(Documentation & Standards)                  |                                                                                                                                      |
| <b>Tools &amp; Ecosystem Integration</b>               |           ...<br>Integration via APIs, SDKs and Automation Scripts |                                                                                                                                        |                                                                                                                                      |                                                                                                                                             |                                                                                                                                            |                                                                                                                                       |                                                                                                                                                     |                                                                                                                                      |
| <b>Data &amp; Knowledge Layer</b>                      | <br>Specs & Standards<br>(IEEE, ISO, etc.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | <br>Design Examples & Best Practices                | <br>Simulation Results & Testbenches             | <br>Failure Cases & Root Cause Data                    | <br>Component & BOM Databases                         | <br>Manufacturing Data & Guidelines              | <br>User Feedback & Learning Data                              |                                                                                                                                      |
| <b>Infrastructure Layer</b>                            | <br>Cloud / On-Prem                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | <br>GPU / CPU Compute                               | <br>Docker / Kubernetes                          | <br>Vector DB                                          | <br>CI/CD & MLOps                                     | <br>Security & Access Control                    | <br>Scalable Architecture                                      |                                                                                                                                      |

### IP STATUS

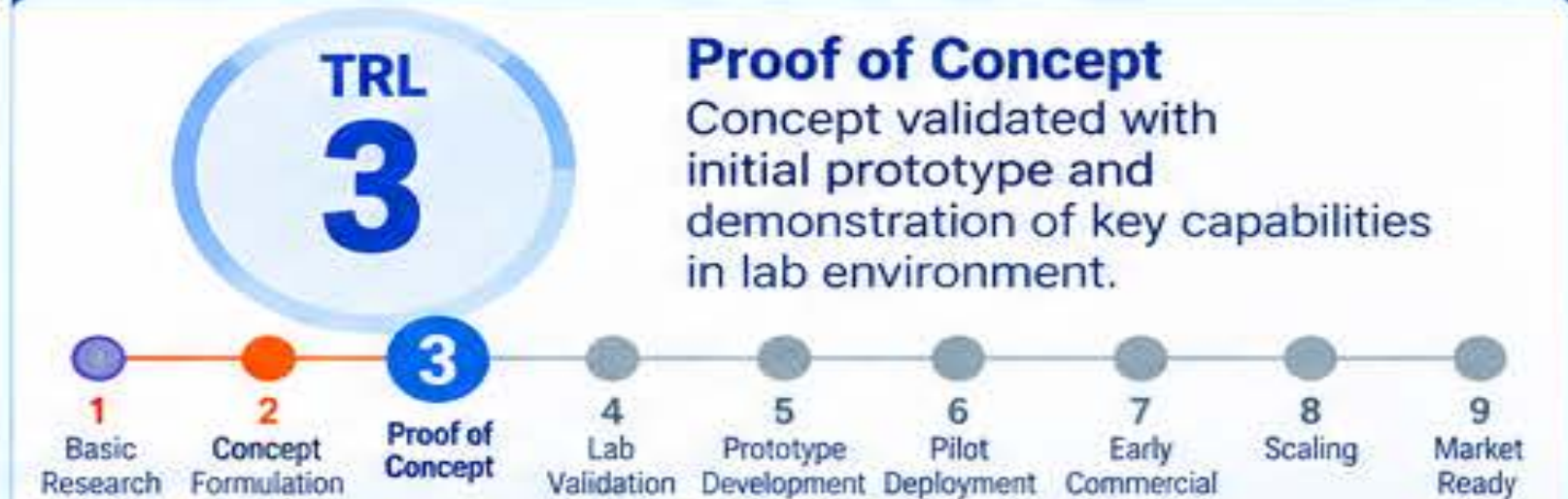

**Planned**

Provisional / Utility Patents planned for key innovations

**Areas of Planned IP**

- ✓ Specification Intelligence (SpecificAI)
- ✓ Automated Spec-to-RTL generation
- ✓ AI-driven verification and testbench generation
- ✓ AI-based PCB design, SI/PI optimization
- ✓ BOM optimization and defect analysis
- ✓ Multi-agent orchestration for EDA workflows

### TECHNOLOGY READINESS LEVEL (TRL)

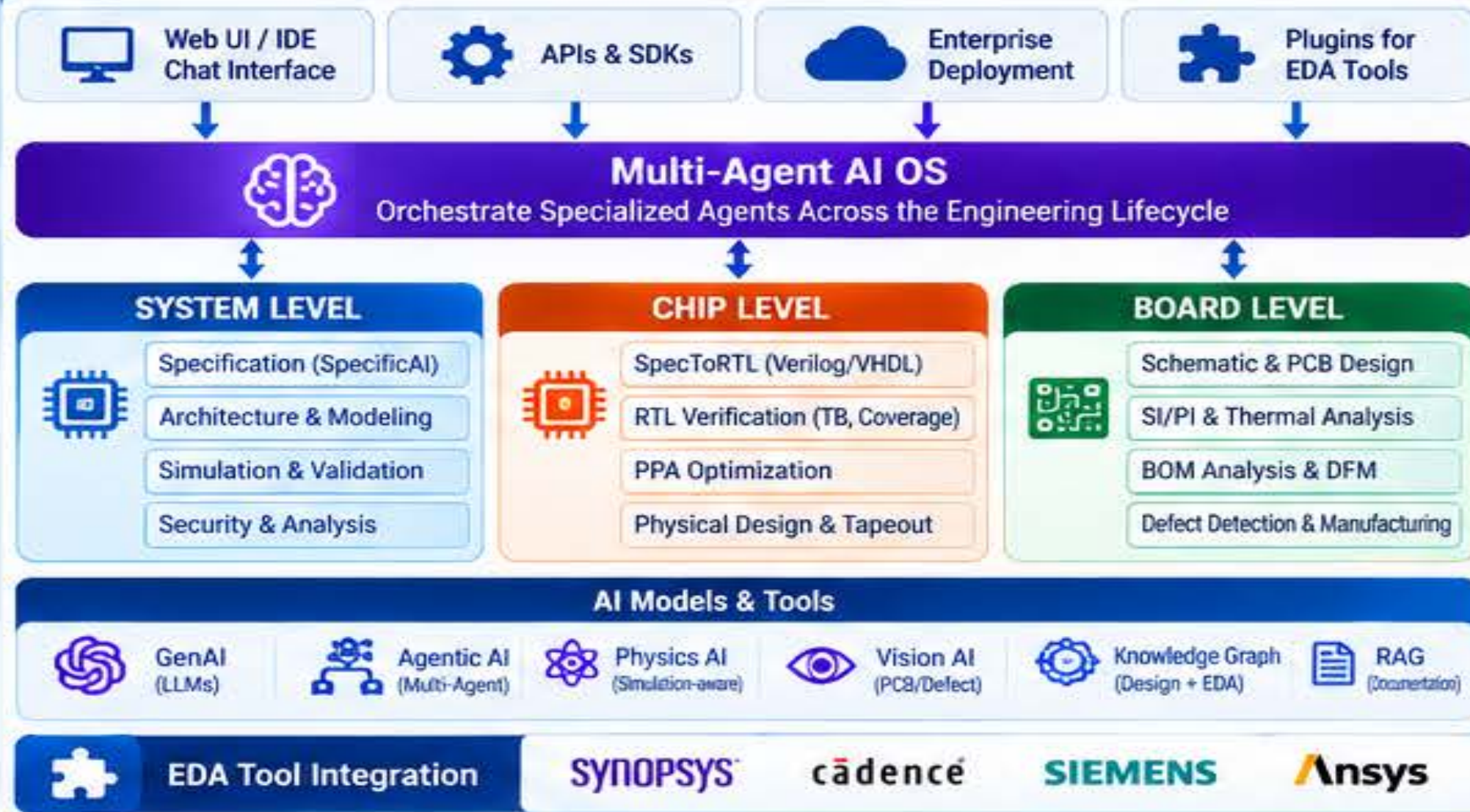


### KEY TECHNOLOGIES USED

|                                                                                                                                                             |                                                                                                                                                     |                                                                                                                                                               |                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <br><b>GenAI (LLMs)</b><br>GPT-4, Llama, Mistral, Domain-specific LLMs | <br><b>Agentic AI</b><br>LangChain, LangGraph, CrewAI, AutoGen | <br><b>Physics AI</b><br>Simulation-aware models for PPA, SI/PI, Thermal | <br><b>RAG &amp; Knowledge</b><br>LlamaIndex, Vector DB, Graph + EDA Knowledge |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|



### 1 PRODUCT ARCHITECTURE



### 2 KEY PRODUCT MODULES



### 3 PROTOTYPE / MVP



### 4 DEMONSTRATIONS

**Specification → RTL Live Demo**

- Natural language spec to Verilog/VHDL

**Verification Demo**

- AI testbench generation
- Simulation & coverage
- Bug detection & fix

**PCB Design Demo**

- Schematic to layout
- DRC/ERC check
- SI/PI analysis

**BOM Analysis Demo**

| Part      | Price  | Availability | Alternate |
|-----------|--------|--------------|-----------|
| MCU       | \$2.50 | In Stock     | ✓         |
| DDR4      | \$8.00 | In Stock     | ✓         |
| PMIC      | \$1.20 | Limited      | ✓         |
| Connector | \$0.80 | In Stock     | ✓         |

- Cost optimization
- Alternatives
- Supply chain analysis

**Defect Detection Demo**

- AI vision-based defect detection
- Root cause analysis
- Suggested fixes

### 5 PILOTS & TRACTION

- Pilot 1: Academic Partner**  
AI Tutor for VLSI/PCB courses (ongoing)  
**50+ students using MVP**
- Pilot 2: PCB Design Company**  
AI-assisted schematic & layout (in progress)  
**Design cycle ~40% faster**
- Pilot 3: Semiconductor Startup**  
Spec-to-RTL and verification pilot (in discussion)  
**Early results positive**
- Pilot 4: EMS / Manufacturing Partner**  
BOM analysis & defect detection (planned)  
**Expected start Q1 2027**

### 6 CUSTOMER DISCOVERY / TARGET USERS



### 7 PARTNERSHIPS & COLLABORATIONS



### 8 CURRENT DEVELOPMENT STATUS



### 1. Prototype / MVP / Product Status

An AI-first, multi-agent EDA platform  
for autonomous semiconductor & PCB design,  
verification and training.

**PRAGYAN AI Copilot**

- Chat to RTL
- Design Assistant
- Verification Agent
- PCB Review Copilot
- Training Copilot
- Project Workspace

**Natural Language to RTL**

Design a 4-bit synchronous counter with enable and reset

**Generate RTL**

**Generated SystemVerilog**

```
module counter_4bit (
    input logic clk, rst, en,
    output logic [3:0] count
);
    always_ff @(posedge clk or
        if (rst) count <= 4'd0;
        else if (en) count <= count + 1'b1;
    endmodule
```

**Simulation & Waveform**

clk, rst, en, count[3:0]

**Verification Coverage**

92%

- Functional
- Assertion
- Code
- Toggle
- FSM

**PCB Review Copilot**

EMI Risk: High

Thermal: Medium

Signal Integrity: Good

DRC: Passed

**AI Training Copilot**

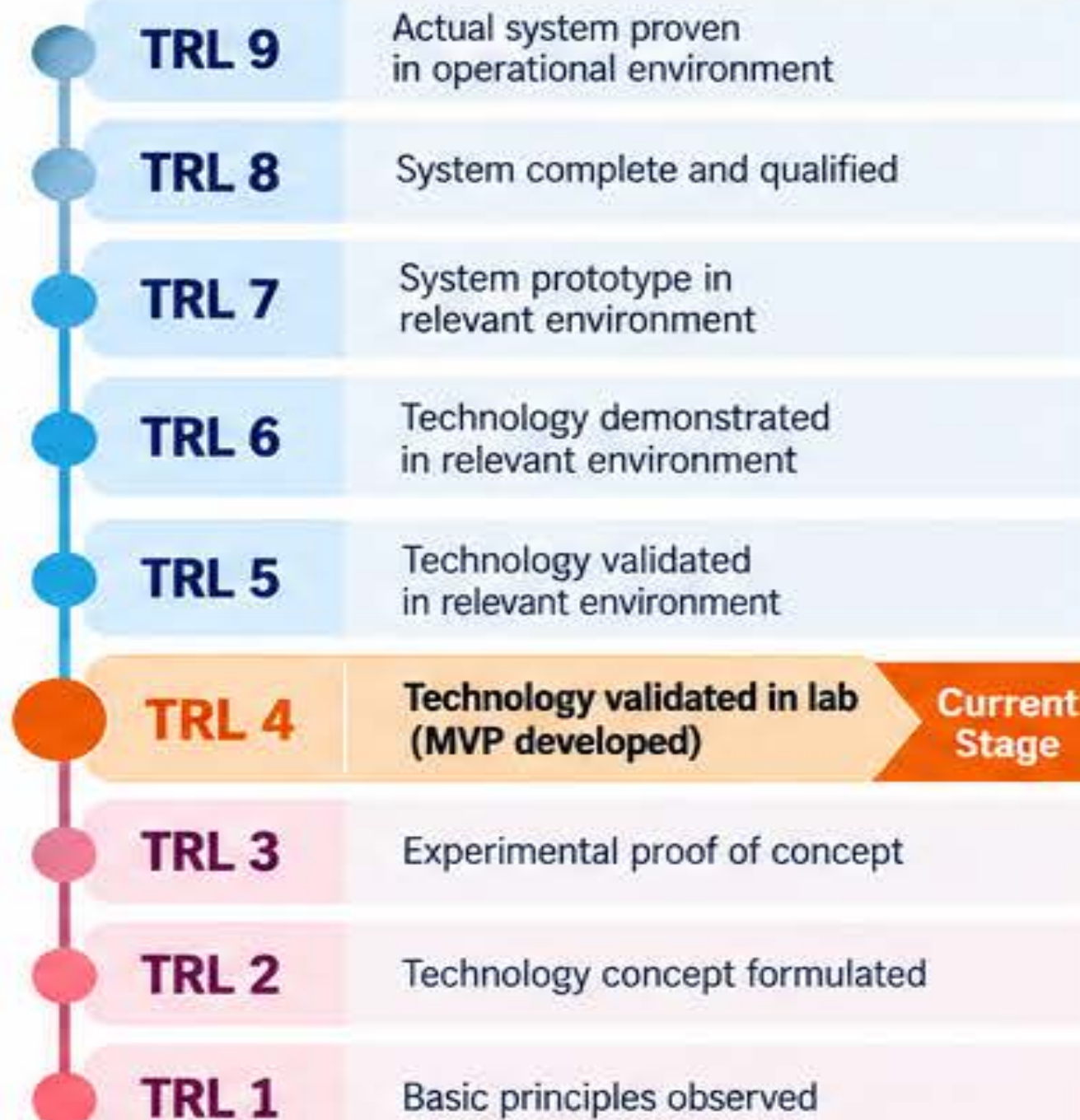
Why is my testbench failing?

Let's debug this together. Can you check the reset sequence and clock timing?

**MVP Developed**

- Core capabilities working in lab environment
- TRL 4 – Validated in Lab (as per internal testing)

### 2. Technology Readiness Level (TRL)



#### Next Steps (12–18 Months)

- Move to TRL 5: Pilot deployments with industry and academic partners
- Validate at customer environments with real design projects

### 3. Pilots / Deployments

Early pilots with academic institutions, MSMEs and industry design teams to validate real-world impact.



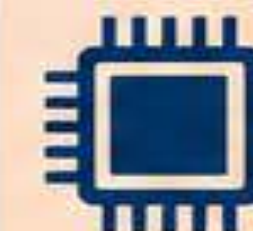
#### Academic Pilot **In Progress**

- Engineering colleges & universities
- AI-powered VLSI/PCB hands-on training (Copilot-Led Lab)
- Validated with student projects and coursework
- Building curriculum integration



#### MSME / Startup Pilot **In Progress**

- Hardware product startups & electronics MSMEs
- Spec-to-RTL generation and verification support
- PCB review and predictive validation
- Reducing design turnaround time and re-spin risk



#### Industry Collaboration **Planned / Early Engagement**

- Semiconductor and electronics design teams
- Evaluation for deployment in real design projects
- Focus on verification automation and waveform intelligence
- Discussions for PoC and enterprise deployment



#### Target Outcomes

- Validate performance, usability and ROI in real scenarios
- Refine product based on pilot feedback
- Scale to TRL 5 and commercial deployment



#### Key Takeaways



MVP ready  
(TRL 4)



Pilots with academia,  
MSMEs and industry  
in progress



Real-world validation  
to reach TRL 5



Clear path to  
commercial deployment

# Product/ Solution - Readiness Level

## Under the Hood: Readiness Level & Defensibility

| Product / Vertical             | Stage                 | TRL Level | Status Description                                                                                                                     |
|--------------------------------|-----------------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------|
| 1. VLSI Front End (RTL Agent)  | Prototype / MVP       | TRL 4     | Validated in Lab. Core "RTL-to-Spec" agent works on isolated modules (e.g., FIFO, UART). Now scaling to subsystem level.               |
| 2. PCB Design (Review Copilot) | Prototype / MVP       | TRL 4     | Validated in Lab. "Risk Auditor" kernels can currently detect specific EMI patterns in static file uploads.                            |
| 3. Talent Engine (Training)    | Live / Early Traction | TRL 6     | Demonstrated in Environment. Curriculum is live; "Applied AI Lab" students are currently using these tools to build internal projects. |

### The Proprietary Data Moat

Generic LLMs scrape the web for finished code.

PragyanAI captures Design Judgment Data—the human rationale behind engineering decisions—harvested directly from live **Consulting Pods**. This process data cannot be scraped by competitors.

# Product/ Solution - Readiness Level



**PragyanAI ElevateNext**  
Multi-Agent Orchestration System

● SYSTEM ONLINE

Mission / Goal

Design a synchronous FIFO module in Verilog. Specifications: Depth=16, Data Width=8 bits. Include a simple testbench.

⌚ Processing...

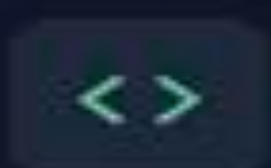
ACTIVE CREW



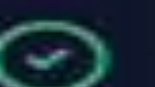
**Researcher**  
Technical Scout



**Analyst**  
Architect



**Engineer**  
Implementation



# Product/ Solution - Readiness Level

>\_ Agent\_Trace\_Logs

```
14:19:42 [System] Initializing CrewAI process...
14:19:42 [Manager] Assigning task to Research Agent: "Design a synchronous FIFO module in Verilog. Specifications: Depth=16, Data Width=8 bits. Include a simple testbench."
14:19:42 [Researcher] Analyzing technical requirements...
14:19:54 [Researcher] Specs gathered. Interface defined.
14:19:54 [Researcher] Key Insight: This document outlines the standard specifications and architectural requirements necessary to design...
14:19:54 [Manager] Handing over specs to Systems Architect.
14:19:54 [Analyst] Designing logic architecture...
14:20:14 [Analyst] Architecture frozen. Logic plan ready.
14:20:14 [Manager] Briefing Lead Engineer for implementation.
```

>\_ Agent\_Trace\_Logs

```
14:19:42 [Researcher] Analyzing technical requirements...
14:19:54 [Researcher] Specs gathered. Interface defined.
14:19:54 [Researcher] Key Insight: This document outlines the standard specifications and architectural requirements necessary to design...
14:19:54 [Manager] Handing over specs to Systems Architect.
14:19:54 [Analyst] Designing logic architecture...
14:20:14 [Analyst] Architecture frozen. Logic plan ready.
14:20:14 [Manager] Briefing Lead Engineer for implementation.
14:20:14 [Writer] Writing code implementation...
14:20:25 [Writer] Implementation complete.
14:20:25 [System] Process finished successfully.
```

# Product/ Solution - Readiness Level

## Mission Output

 Copy

As a Lead Engineer, I have translated the detailed architectural plan into the RTL implementation for the `sync\_fifo` module. This design correctly utilizes the 5-bit pointer logic necessary to handle the 16-entry depth and distinguish between full and empty states.

## Verilog Implementation

VERILOG

```
/**
 * Synchronous FIFO (First-In, First-Out) Implementation
 * Depth: 16 entries (DEPTH_LOG2 = 4)
 * Pointer Width: 5 bits (DEPTH_LOG2 + 1)
 *
 * Uses extra pointer bit (MSB) to distinguish between Full and Empty.
 * - Empty: wr_ptr == rd_ptr (All 5 bits match)
 * - Full: Address bits match, MSBs differ.
```



# Product/ Solution - Readiness Level

```
// **Power Rails & Distribution**
NET VBUS (5V_Input) {
    J1.VBUS -> D1.A
    D1.C -> U3.VIN (Charger Input)
    D1.C -> U2.VIN (LDO Input)
    D1.C -> C_BULK_IN+
    // Physical Assignment: Wide Trace L1, transition to L3 Power Plane.
}

NET VBAT (Battery Power) {
    J2.BAT+ -> U3.BAT (Charger Output)
    U3.BAT -> U2.VIN (Alternative Input for LDO)
    // Physical Assignment: L3 Power Plane / 15 mil trace width priority.
}

NET 3V3_MCU (Regulated Power) {
    U2.VOUT -> C1, C2, C3 (Decoupling)
    U2.VOUT -> U1.VCC (ESP32 Supply)
    U2.VOUT -> J3.VCC
    // Physical Assignment: Dedicated pour on L3. Short spokes on L1 to components.
}

NET GND {
    All Grounds -> L2 (Solid Reference Plane)
    // Physical Assignment: L2 is continuous GND. Stitching Vias (L1/L4 to L2) under all components.
}

// **High-Speed Differential Pair (L1)**
NET USB_DP {
    J1.DP -> U1.DP
    // Constraint: Route on L1, 5 mil width, 90 Ohm differential with USB_DM, length matched.
}

NET USB_DM {
    J1.DM -> U1.DM
    // Constraint: Route on L1, 5 mil width, 6 mil gap to USB_DP, referenced to L2.
}

// **RF Critical Net (L1)**
NET ANTENNA {
    U1.RF_OUT -> Antenna Connector / Trace Antenna Feed Point
    // Constraint: Route on L1 only. 7 mil width (50 Ohm SE). Isolation required.
}

// **Digital Control (L1/L4)**
NET DATA_DHT {
    U1.GPIO -> R2.PAD1
    R2.PAD2 -> 3V3_MCU
    U1.GPIO -> J3.DATA
    // Constraint: Route away from USB/RF. R2 placed adjacent to U1.
}
```

# Product/ Solution - Readiness Level



**PragyanAI ElevateNext**

Hardware Design Automation

● EDA TOOLS ACTIVE

## 3. Critical Fabrication Notes

These notes specify the mandatory material, processing, and finishing requirements essential for achieving the required signal integrity and reliability, especially concerning RF and impedance control.

### A. Manufacturing Specifications

1. **Board Dimensions & Thickness:** Total thickness must be maintained at **1.57 mm (62 mils)**, using standard FR4 materials.
2. **Copper Weight:** 1 oz (35  $\mu\text{m}$ ) copper required for all four layers (L1, L2, L3, L4).
3. **Surface Finish:** **ENIG (Electroless Nickel Immersion Gold)** finish required. This ensures a planar surface essential for reliable soldering of fine-pitch components (U1) and provides superior contact quality for the RF antenna pad.
4. **Solder Mask:** Green standard solder mask (or matte black if aesthetic specification requires).



# Product/ Solution - Readiness Level



**PragyanAI ElevateNext**

Hardware Design Automation

● EDA TOOLS ACTIVE

5. **\*\*Silkscreen:\*\*** White top/bottom standard silkscreen.

## **B. Controlled Impedance Requirements**

1. **\*\*Impedance Tolerance:\*\*** The manufacturer must verify and meet impedance targets within the specified tolerance. A TDR coupon (test coupon) is mandatory for verification of both 50  $\Omega$  single-ended and 90  $\Omega$  differential lines.

2. **\*\*50  $\Omega$  Single-Ended:\*\*** Targeted on L1 (ANTENNA net). **\*\*Width: 7 mils\*\***, referenced to L2 (GND) at a separation of 8 mils. Tolerance  $\pm 5\%$ .

3. **\*\*90  $\Omega$  Differential:\*\*** Targeted on L1 (USB\_DP/DM nets). **\*\*Width: 5 mils, Gap: 6 mils\*\***, referenced to L2 (GND) at a separation of 8 mils. Tolerance  $\pm 7\%$ .

4. **\*\*Stackup Verification:\*\*** The manufacturer must confirm the final prepreg/core thicknesses and the material  $E_r$  values, providing a calculated impedance report prior to etching.

# Product/ Solution - Readiness Level



**PragyanAI ElevateNext**

Hardware Design Automation

EDA TOOLS ACTIVE

referenced to L2 (GND) at a separation of 8 mils. Tolerance  $\pm 1\%$ .

4. **\*\*Stackup Verification:\*\*** The manufacturer must confirm the final prepreg/core thicknesses and the material  $E_r$  values, providing a calculated impedance report prior to etching.

## C. Mechanical and Thermal Requirements

1. **\*\*Via Processing:\*\*** **\*\*Power and Thermal Vias\*\*** (specifically beneath U2 and U3 thermal pads, and VBUS/VBAT/3V3 vias carrying high current) must be **\*\*Vias In Pad (VIP)\*\*** and **\*\*filled/capped\*\*** to prevent solder wicking and ensure reliable thermal transfer to the internal planes (L2/L3).
2. **\*\*RF Keep-out Zone:\*\*** The defined antenna clearance zone (150 mils from the radiating element) must be maintained across **\*\*all four layers (L1, L2, L3, L4)\*\***. No copper (flood, traces, vias) is permitted in this zone.
3. **\*\*GND Stitching:\*\*** Ensure liberal placement of stitching vias connecting L1, L4, and L2 (GND) every  $\lambda/20$  (or roughly 150–200 mils) around the perimeter and near high-speed nets to maximize EMI shielding and minimize ground loop inductance.

# Product/ Solution - Readiness Level

app

Knowledge Base

**Spec Designer**

Spec Chat

RTL Generator

Verification Bench

## PragyanAI RTL Design Specification Generator

Architect's Draft

### RTL Design Specification (RDS) for AXI based 16-Bit Multiplier

1. Functional Overview

The AXI based 16-Bit Multiplier is a digital circuit that performs multiplication of two 16-bit unsigned integers. The module is designed to be integrated into a System-on-Chip (SoC) and communicates with other modules through the AXI (Advanced eXtensible Interface) protocol. The purpose of this module is to provide a high-performance multiplication operation for various applications, such as digital signal processing, image processing, and machine learning.

2. Interface Control Document (ICD)

| Name          | Dir | Width | Desc                    | Protocol |
|---------------|-----|-------|-------------------------|----------|
| s_axi_awaddr  | I   | 32    | AXI write address       | AXI      |
| s_axi_awvalid | I   | 1     | AXI write address valid | AXI      |

Critic's Audit

Technical Audit Report

1. Introduction

The provided RTL Design Specification (RDS) for the AXI-based 16-Bit Multiplier has been reviewed for potential "design killers" in the areas of CDC Hazards, Reset Integrity, Protocol Violations, and Resource Efficiency.

2. CDC Hazards

- The RDS mentions a 2-FF synchronization strategy for clock domain crossing (CDC). However, it does not provide details on how this strategy is implemented or which signals are synchronized.
- RECOMMENDATION:** Provide a detailed description of the CDC strategy, including the specific signals that are synchronized and the implementation of the 2-FF synchronization.
- RISK LEVEL:** Medium

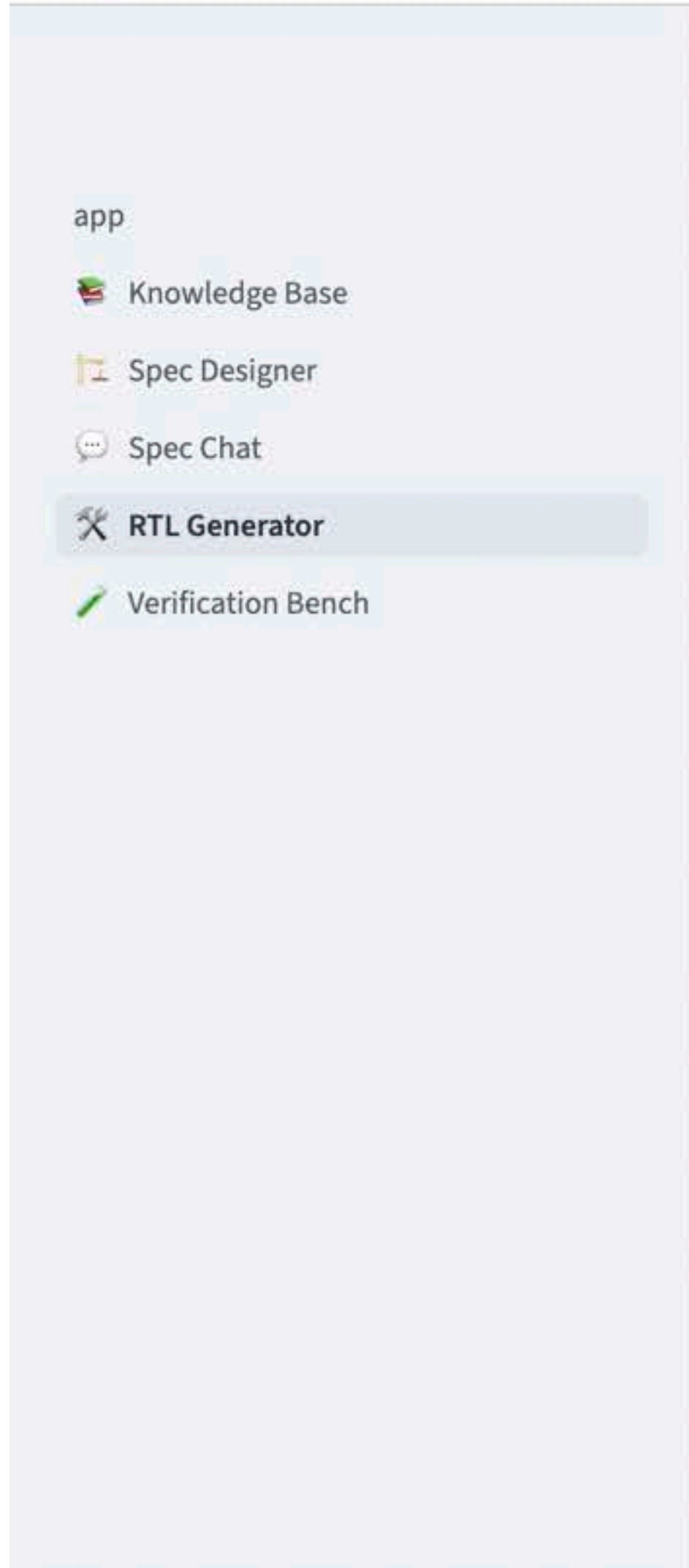
3. Reset Integrity

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Manage app







### Generate Synthesizable Verilog/VHDL from RTL Design Specifications (RDS)

Target Language: 

 **Tip:** Ensure your RDS includes a clear Port List and Clock/Reset strategy for best results.

Upload RDS Specification (.md)

Paste RDS Content Here:

### 1. Functional Overview

### ### 2 Interface Control Document (ICD)

# Product/ Solution - Readiness Level

Share    ⋮

app

 Knowledge Base

 Spec Designer

 Spec Chat

 RTL Generator

 Verification Bench

## Generated Verilog

Here is the Verilog code that implements the AXI base 

```
``verilog
// Import necessary modules
`timescale 1ns/1ps

// Define the module
module axi_multiplier (
    // AXI interface
    input wire      axi_clk,
    input wire      axi_rstn,
    input wire [31:0] axi_awaddr,
    input wire      axi_awvalid,
    output wire     axi_awready,
    input wire [15:0] axi_wdata,
    input wire      axi_wvalid,
    output wire     axi_wready,
    output wire     axi_bvalid,
    input wire      axi_bready,
    input wire [31:0] axi_araddr,
    input wire      axi_arvalid,
    output wire     axi_arready,
    output wire [31:0] axi_rdata,
    output wire     axi_rvalid,
```

## Design Audit Report

### Audit Report

The provided Verilog code implements an AXI-based 16-bit multiplier. After reviewing the code, several potential issues have been identified:

### 1. Combinational Loops or Unintentional Latches

- **CRITICAL:** The `axi_awready`, `axi_wready`, `axi_bvalid`, `axi_arready`, and `axi_rvalid` signals are assigned values in the `always @(posedge axi_clk)` block without considering the current state of the FSM. This can lead to combinational loops or unintentional latches. To fix this, the assignments should be moved inside the FSM's state transitions.
- **CRITICAL:** The `result_reg` signal is assigned a value in the `always @(posedge axi_clk)` block without considering the current state of the FSM. This can lead to combinational loops or unintentional latches. To fix this, the assignment should be moved inside the FSM's state transitions.

# Product/ Solution - Readiness Level

app

Knowledge Base

Spec Designer

Spec Chat

RTL Generator

Verification Bench

pragyanai-frontenddesignspecification.streamlit.app/RTL\_Generator

Relaunch to update

Share

Human-in-the-Loop Refinement

Address audit concerns or request architectural changes:

Enter suggestions (e.g., 'Use a behavioral 32-bit adder instead'):

Apply Refinements & Finalize

Golden RTL Generated!

Golden RTL Code

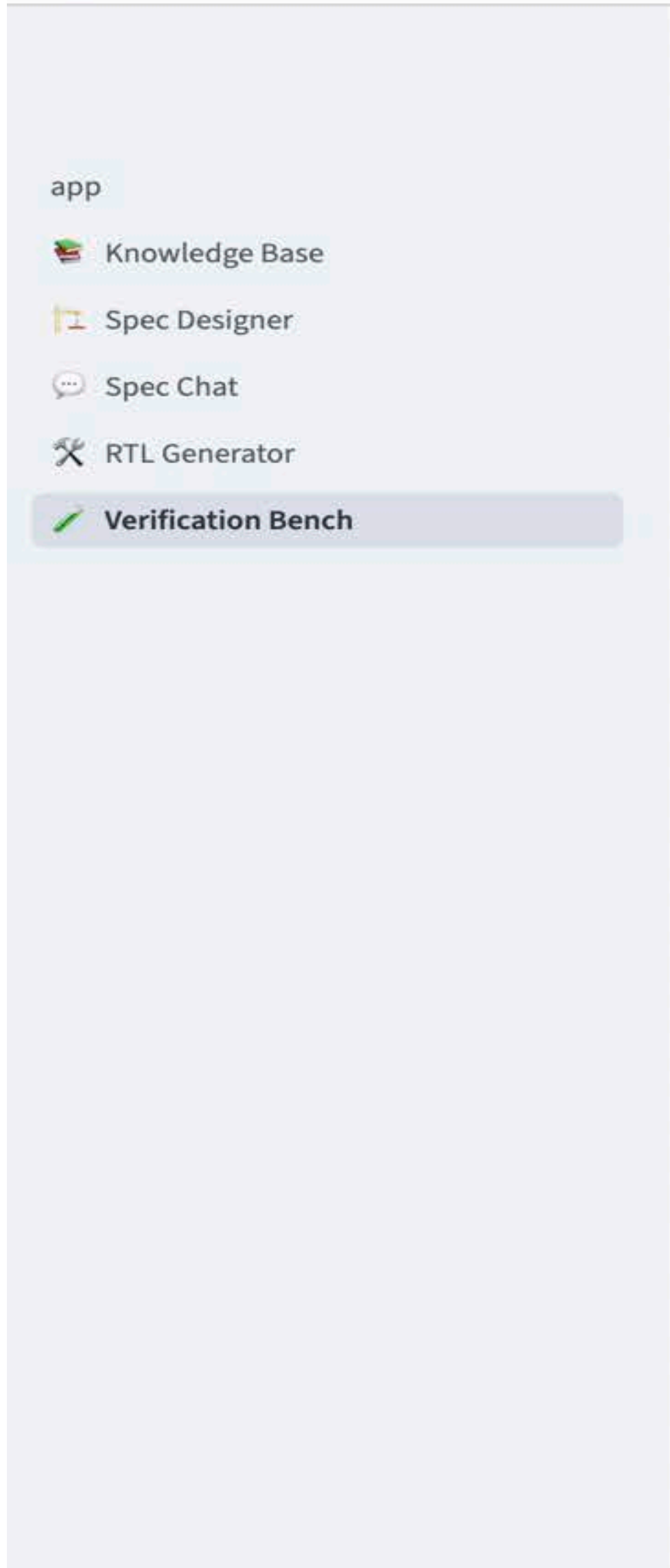
Finalized Code

The provided Verilog code implements an AXI-based 16-bit multiplier. After reviewing the code and addressing the issue:

```
```verilog
// Import necessary modules
`timescale 1ns/1ps

// Define the module
module axi_multiplier (
    // AXI interface
    input wire    axi_clk,
```

Manage app



## 🤔 Test Case Rationale

## Corner Cases

- ## Functional Coverage

- 

# Product/ Solution - Readiness Level

←

→

↺

pragyanai-frontenddesignspecification.streamlit.app/Verification\_Bench

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☰

Relaunch to update

📦

IRIS

Dashboard

Lab Assignment 3...

LIVE TV 24x7: Rep...

Inbox (27) - satee...

Deep Learning

Klassroom - Premi...

Downloadable: Ch...

MIT Deep Learnin...

>>

All Bookm

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🔄

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Knowledge Base

Spec Designer

Spec Chat

RTL Generator

Verification Bench

```
initial begin
    // Test case 1: Zero operands
    inject_stimulus(16'd0, 16'd0, 1'b1);
    #1000;

    // Test case 2: Maximum operands
    inject_stimulus(16'hFFFF, 16'hFFFF, 1'b1);
    #1000;

    // Test case 3: Overflow
    inject_stimulus(16'h7FFF, 16'h7FFF, 1'b1);
    #1000;

    $finish;
end
endmodule
...

This testbench includes the following features:
```

1. **Clock generator**: A 100MHz clock generator is implemented using an `initial` block and a `forever` loop.

2. **Reset logic**: A reset logic is implemented using an `initial` block, which sets the `axi_rstn` signal to 0 for

3. **Stimulus injection**: A task `inject_stimulus` is defined to inject stimulus into the design. This task takes the

4. **Scoreboarding**: A scoreboarding mechanism is implemented using an `always` block, which checks if the result from

5. **Test cases**: Three test cases are implemented in the `initial` block: zero operands, maximum operands, and over

This testbench provides a comprehensive verification environment for the AXI-based 16-bit multiplier design, covering

Download Verilog Testbench

<

Manage a

## 1 Balanced Business Model (Services + Product)

### Services (Revenue Now)

- Skilled resources
- Training & consulting
- Solution outsourcing

### Products (Scalable Growth)

- AI-native tools
- Verification intelligence
- Autonomous workflows

- ✓ Near-term revenue from services
- ✓ Funds product development
- ✓ Sustainable long-term growth

## 2 Domain-Specific AI with LLM Fine-Tuning

- LLM fine-tuned on semiconductor/EDA domain (specs, RTL, UVM, DFT, manufacturing, failure data).
- Better accuracy and relevance than general-purpose LLMs.
- Retrieval-augmented generation (RAG) with hardware knowledge graphs.
- Continuously improves from user data and verification cycles.



Domain Fine-Tuned LLM

- Specs & Standards
- RTL / UVM
- Verification Logs
- Manufacturing Data
- Knowledge Graphs

## 3 End-to-End Comprehensive Solution (Integrates with Existing Tools)

- Covers the complete flow: spec → design → verification → debug → sign-off → manufacturing.
- Integrates with industry-standard tools (Cadence, Synopsys, Siemens, Ansys, etc.).
- Adds AI layer without disrupting existing workflows.
- Unified platform with multi-agent automation, knowledge graphs and analytics.
- Modular deployment – adopt step-by-step or full-stack.

Your Existing EDA Tools

PragyanAI AI Layer

Enhanced Autonomous Workflow

## 4 Affordable & Accessible

- Significantly lower cost than legacy tools.
- Freemium verification pilot for easy adoption.
- Subscription-based platform (₹1K–2K/month + LLM token cost).
- Cost-effective skilling, training and tooling for startups, MSMEs, colleges and R&D teams.



Low Entry Cost



Freemium Pilot



Affordable for Startups & Academia

## 6 Proprietary & Continuously Learning Data Moat

- Every verification run, debug cycle and user interaction generates valuable data.
- Builds the largest AI-native hardware failure & verification intelligence system.
- Includes defect patterns, EMI/thermal risks, manufacturing insights and debugging graphs.
- Data improves models, tools and recommendations over time.



Unique Dataset  
→ Better AI  
→ Higher Value

## 7 Expert Founding Team



- Deep industry experience in VLSI, embedded systems and product engineering.
- Strong AI expertise with PhD and research background.
- Proven track record in building innovative solutions and establishing businesses.
- Committed, passionate and execution-focused team.

## 5 Skilling + Ecosystem Enablement

- Trains next generation engineers in VLSI, PCB and AI.
- Provides skilled resources to industry at affordable cost.
- Collaborates with colleges, government and industry associations.
- Builds an AI-ready semiconductor workforce ecosystem.



Skilled Talent Pipeline



Colleges & Universities



Government Programs



Industry Associations



Internships & Mentorship

## 8 Open & Extensible Ecosystem



- Leverages and integrates with open-source EDA infrastructure (e.g., KiCad, Verilator, OpenROAD, Yosys).
- Open APIs and modular architecture.
- Enables collaboration with startups, academia and industry.
- Fosters an ecosystem of innovation around PragyanAI.



The PragyanAI Advantage



Domain-focused AI (not generic)



Affordable & Accessible



End-to-End Integration



Service + Product for Sustainable Revenue



Proprietary Data Moat



Skilling & Ecosystem



Scalable Global Impact



# Product/ Solution - Impact

## Target Impact & Success Metrics

| Metric                        | Target   |
|-------------------------------|----------|
| Specification Generation Time | ↓ 80%    |
| Architecture Exploration Time | ↓ 70%    |
| RTL Development Effort        | ↓ 60%    |
| Verification Effort           | ↓ 70%    |
| Coverage Closure Time         | ↓ 80%    |
| End-to-End Design Cycle       | ↓ 50–70% |
| Engineering Productivity      | 5–10×    |
| Human Review Accuracy         | >95%     |
| Platform Automation           | >80%     |

## Quantifiable Outcomes

| Parameter                        | Expected Impact         |
|----------------------------------|-------------------------|
| Design Cost Reduction            | 40–60%                  |
| Verification Cost Reduction      | 50–70%                  |
| Bug Reduction                    | 70–90%                  |
| Design Cycle Reduction           | 50–70%                  |
| Engineering Productivity         | 5–10×                   |
| Coverage Closure Effort          | 70–90%                  |
| Student Learning Curve Reduction | 50–70%                  |
| Industry Readiness Improvement   | 3–5× Faster             |
| First-Pass Silicon Success       | Significant Improvement |

# HIGH-VALUE JOB CREATION & NATIONAL IMPACT

Building a Self-Reliant, Sustainable & Equitable Semiconductor Ecosystem from Karnataka

## 1 HIGH-VALUE JOB CREATION IN KARNATAKA (BEYOND BENGALURU)

### THE PROBLEM



Currently, high-paying VLSI & AI jobs are concentrated solely in Bengaluru, leading to migration and regional disparity.

### OUR SOLUTION



We are establishing "Applied AI Labs" in engineering colleges across Tier-2 & Tier-3 cities.

Targeting:

HUBBALLI MYSURU BELAGAVI

### DIRECT SOCIAL IMPACT



#### From "Unemployable" to "Elite"

We transform fresh graduates from local colleges into "Deep-Tech Architects" capable of working on global semiconductor projects.



#### Wealth Distribution

By enabling students to work on high-value "Consulting Pods" from their college campuses, we bring Bengaluru-level salaries to Tier-2 cities, boosting the local economy.



#### TARGET

500+ Deep-Tech Jobs  
in North Karnataka within 3 years.



## 2 SUPPORT FEW STARTUPS – LAUNCH ELECTRONICS PRODUCTS SOVEREIGN CAPABILITY (MAKE IN INDIA & IMPORT SUBSTITUTION)



### Strategic Independence

Currently, India's chip design ecosystem is 100% dependent on expensive, foreign-licensed EDA tools (Synopsys/Cadence).

We are building the indigenous "Intelligence Layer" for India's Semiconductor Mission.

Initial face design and verification one can use PragyanAI solution and later they leverage EDA Tools for short period – single licence for large.



### Economic Benefit for Startups

- Democratising Design:** Our "Agentic EDA Kernels" lower the barrier to entry, enabling small Indian hardware startups to design chips locally at 1/10th the cost of global licenses.
- Retaining IP in India:** Instead of Indian talent building IP for US companies, our "Venture Studio" model ensures that Intellectual Property (IP) remains in India, owned by Indian founders.

### SUPPORTED STARTUPS ECOSYSTEM



Low-cost EDA  
Access



Faster Design  
Cycles



Indigenous IP  
Ownership



Global-Ready  
Products

### OUTCOME



A self-reliant India in Semiconductor Design, reducing import dependency and creating global competitiveness.

ATMANIRBHAR BHARAT • MAKE IN INDIA

## 3 ENVIRONMENTAL SUSTAINABILITY (REDUCING ELECTRONIC WASTE)



### Reducing "Re-Spins"

A major source of global e-waste is failed PCB prototypes (re-spins) due to design errors.



### Impact

Our "PCB Review Copilot" predicts thermal and EMI failures virtually before manufacturing begins.



### Result

This prevents the physical scrapping of thousands of defective circuit boards, directly aligning with SDG 12 (Responsible Consumption and Production).



SUSTAINABLE DESIGN. SMARTER PLANET. STRONGER FUTURE.

### ENVIRONMENTAL IMPACT (3 YEARS)



10,000+

PCB Re-spins Prevented



50+

Tons of E-waste Reduced



Lower Carbon Footprint  
through smarter design  
& fewer physical prototypes

## 4 QUANTIFIABLE IMPACT METRICS (PROJECTION FOR 3 YEARS)



### TALENT

1,000+

Students trained in  
Agentic AI & VLSI

### Across 5+ Partner Colleges

- DSCE, Bengaluru
- Vidhya Vikas Institute of Engg., Mysuru
- GNDCE, Bidar
- VVIT, Mysuru
- SB University, Dharwad
- GIT, Belagavi



### INNOVATION

20+

Indian Startups  
Supported

With low-cost "Agentic EDA" tools,  
mentorship & venture support



### REGIONAL GROWTH

₹10 Cr+

In direct salary wealth  
generated in Tier-2/3  
Karnataka cities

Boosting local economies in  
Hubballi, Mysuru, Belagavi  
& surrounding regions

### THE BIGGER PICTURE



- ✓ Retain Talent in Karnataka
- ✓ Build Global-Ready Deep-Tech Talent from Tier-2/3 Cities
- ✓ Create Sustainable Jobs & Wealth
- ✓ Strengthen India's Semiconductor Sovereignty



We are not just building a company; we are building an ecosystem that creates jobs, supports startups, protects the planet, and powers India's semiconductor future.



| Dimension                                | Cadence Design Systems   | Synopsys                 | Siemens EDA (Mentor)     | Ansys                                 | Altium                | Open Source (KiCad, Verilator, OpenROAD, Yosys) | PragyanAI                                    |
|------------------------------------------|--------------------------|--------------------------|--------------------------|---------------------------------------|-----------------------|-------------------------------------------------|----------------------------------------------|
|                                          |                          |                          |                          |                                       |                       |                                                 |                                              |
| Target Market Focus                      | Large enterprises        | Large enterprises        | Large enterprises        | Simulation & physics (multi-industry) | PCB designers (MSMEs) | Early-stage, research, academia                 | Enterprises + MSMEs + Startups + Academia    |
| Cost / Licensing                         | ✗ Very High              | ✗ Very High              | ✗ High                   | ✗ High                                | — Moderate            | ✓ Free (Open Source)                            | ✓ Affordable SaaS & Flexible Models          |
| AI-Native & Autonomous Workflows         | ✗ Limited (AI add-on)    | ✗ Limited (AI add-on)    | ✗ Limited (AI add-on)    | ✗ Limited                             | ✗ Minimal             | ✗ None                                          | ✓ Yes (Multi-Agent AI)                       |
| Spec-to-RTL Generation                   | ✗ No                     | ✗ No                     | ✗ No                     | ✗ No                                  | ✗ No                  | ✗ No                                            | ✓ Yes (Natural Language to RTL)              |
| Verification Intelligence & Debugging    | — Limited                | — Partial                | — Partial                | ✓ Strong Simulation (Physics)         | ✗ No                  | ✗ Basic                                         | ✓ Yes (Autonomous Debug & Waveform Analysis) |
| PCB Design AI (DFM/DFT/EMI/Thermal)      | — Partial (High-end)     | — Partial (High-end)     | — Partial                | ✓ Strong (Physics/EMI/Thermal)        | ✗ Basic               | ✗ None                                          | ✓ Yes (Predictive PCB Review Copilot)        |
| Interactive AI Tutor & Training Platform | ✗ No                     | ✗ No                     | ✗ No                     | ✗ No                                  | ✗ No                  | — Community resources                           | ✓ Yes (Copilot-Led Lab)                      |
| Cloud-Native & API Ecosystem             | — Limited                | — Limited                | — Limited                | — Partial                             | — Partial             | ✓ Yes (Self hosted)                             | ✓ Yes (Cloud-native, API-first)              |
| Ease of Adoption                         | ✗ Complex, expert-driven | ✗ Complex, expert-driven | ✗ Complex, expert-driven | — Moderate                            | ✓ Easy (PCB)          | — Moderate (steep learning)                     | ✓ Easy (Natural language, guided)            |



## Why PragyanAI Wins



**1. Democratizes** Semiconductor & PCB Design with AI-native, autonomous workflows at affordable cost.



**2. Serves underserved** MSMEs, startups and academic institutions, in addition to large enterprises.



**3. Unique combination** of Spec-to-RTL, verification intelligence, predictive PCB review and AI training platform.



**4. Builds on open-source** EDA ecosystem with proprietary AI intelligence layer (domain-specific).



**5. Faster design cycles,** fewer re-spins, **lower cost** and skilling the next generation of engineers.

## 1. Target Customers / Users

Across the semiconductor and electronics value chain

### Semiconductor Design Companies (Fabless)



- ASIC & SoC design teams
- Product engineering teams
- Startups & scaleups

**Need:** Faster, accurate design & verification

### Electronics & PCB Design Houses



- EMS companies
- Industrial electronics firms
- Consumer electronics OEMs
- Automotive & IoT hardware firms

**Need:** Predictive PCB validation to avoid costly re-spins

### Academic & Training Institutions



- Engineering colleges
- Universities & research labs
- Skill development programs

**Need:** AI-driven hands-on VLSI/PCB learning and debugging

### MSMEs & Product Startups



- Hardware product startups
- IoT & embedded system firms
- MSMEs entering electronics

**Need:** Affordable, easy-to-use AI design assistance

### System Integrators & OEMs



- Automotive, Aerospace, Industrial
- Defence & Space electronics
- Consumer electronics OEMs

**Need:** Reliable, faster design cycles with lower risk

### Government & Research Labs



- ISRO, DRDO, DER, CDAC
- National semiconductor programs
- Centres of Excellence

**Need:** Build indigenous EDA and design intelligence

## 2. Market Opportunity

The global EDA and PCB design ecosystem is large and growing, with a major opportunity for AI-native, autonomous solutions.

**\$14.5B**  
Global EDA Market (2024)

Growing at 9.8% CAGR to reach **\$26.3B** by 2030

**\$9.2B**  
Global PCB Design Tools Market (2024)

Growing at 8.5% CAGR to reach **\$15.1B** by 2030

**\$3.1B**  
Engineering Training & EdTech (Tech Skills, 2024)

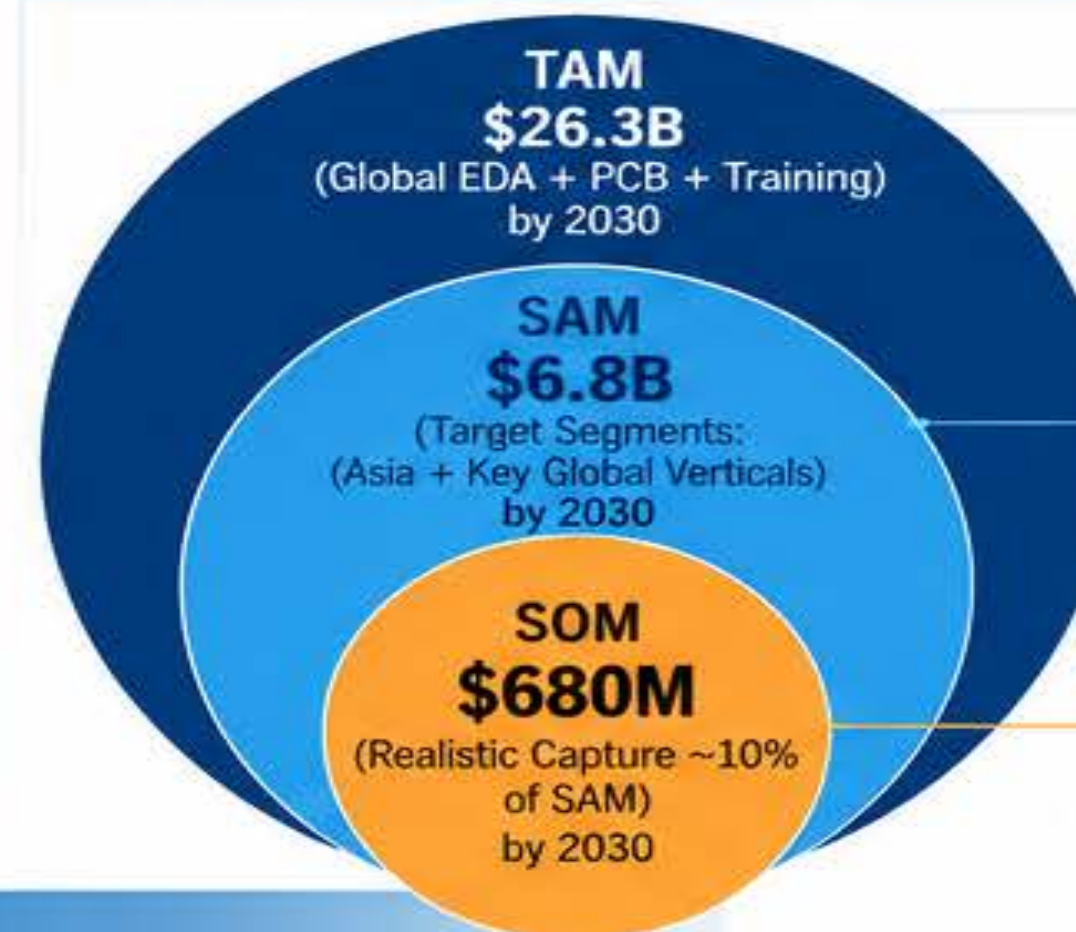
Growing at 12.6% CAGR to reach **\$6.3B** by 2030

**\$50B+**  
India Semiconductor Market (2030 Target)

Driven by govt. initiatives and growing electronics manufacturing

## 3. TAM / SAM / SOM (5+ Year View)

**TAM** – Total Addressable Market  
**SAM** – Serviceable Addressable Market  
**SOM** – Serviceable Obtainable Market



**TAM: \$26.3 Billion**

- Global EDA: \$26.3B (2030)
- Global PCB Design Tools: \$15.1B (2030)
- Engineering Training (Tech Skills): \$6.3B (2030)
- Total Addressable Market: ~\$26.3B+

**SAM: \$6.8 Billion**

- Focus on Asia (India, Southeast Asia) + key global verticals (Automotive, Industrial, Aerospace, Consumer)
- ~25% of global market
- Serviceable Addressable Market: ~\$6.8B

**SOM: \$680 Million**

- Realistic capture ~10% of SAM over 5+ years
- Driven by strong India adoption, strategic partnerships and global expansion
- Serviceable Obtainable Market: ~\$680M

## 4. Key Drivers for Market Growth



Growing semiconductor and electronics manufacturing in India and globally



Shortage of skilled VLSI/PCB engineers



Need for faster time-to-market



High cost of design errors and re-spins



Rising adoption of AI in engineering workflows



Strong government support (India Semiconductor Mission)

# Business Model & Growth Strategy

**PRAGYAN AI**

AI, Agentic AI EDA Kernel for Autonomous Semiconductor Design & Verification

## Business Model & Revenue Strategy

Skilling → Skilled Resources → Outsourcing → Platform Revenue

Building the Autonomous Engineering Office for India's Semiconductor Mission.



### TARGET CUSTOMERS / USERS

- Semiconductor Companies** (Design & Verification Teams)
- Hardware Startups & MSMEs** (Chips, PCB, IoT Products)
- Academic Institutions** (Engineering Colleges & Universities)
- Government & R&D Labs** (Semiconductor Mission, ESDM)
- PCB Design & Electronics Manufacturing Companies**

### PRAGYAN AI Platform



### REVENUE STREAMS

- 1 Platform-based Revenue (SaaS / APIs)**
  - Monthly subscription (₹1K – 2K) per user (excluding LLM token cost)
  - Modules: RTL, Verification, PCB Review, AI Tutor, Debug Intelligence
  - Freemium + Paid tiers
  - Starts Generating Significant Revenue (Year 2+)**
- 2 Skilled Resources Revenue**
  - Provide trained VLSI / Verification / PCB engineers
  - Affordable pricing for startups, MSMEs and enterprises
  - Generation Starts Immediately (Year 1)**
- 3 Outsourcing / Project Revenue**
  - Design verification, PCB review, RTL development, testbench creation
  - End-to-end project support
  - Affordable and faster turnaround
  - Generation Starts Immediately (Year 1)**

### 4 Verification Pilots (Free / Freemium)

- Select pilots for startups, MSMEs, colleges and government projects
- Free or freemium to build product usage, case studies and dataset moat
- Convert to paid subscriptions after success

### 5 Skilling in VLSI & PCB (Till platform revenue scales)

- 6–12 month industry aligned programs
- Train students, freshers and working professionals
- Build pipeline of skilled resources for our own needs, client projects and outsourcing
- Helps fund operations until platform revenue grows

### PARTNERSHIPS & COLLABORATIONS

- Government**
  - Semiconductor Mission, ESDM initiatives
  - Pilot projects, grants, incubation support
- Colleges & Universities**
  - Curriculum integration, AI Copilot labs
  - Faculty & student training, joint research
- Hardware Technology Associations**
  - Industry connect, use cases, dataset access
  - Co-marketing, events, ecosystem growth

### PRICING STRATEGY (Very Low Entry Price)

- Platform (SaaS)**
  - ₹1,000 – ₹2,000 per user per month (excluding LLM tokens)
  - Freemium → Paid
- Skilled Resources**
  - Affordable pricing for trained engineers (VLSI / Verification / PCB)
  - Flexible engagement models
- Outsourcing / Projects**
  - Cost-effective project pricing for startups, MSMEs and enterprises

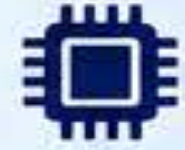
### REVENUE TIMELINE



### KEY OUTCOMES

- Immediate Revenue** → From skilled resources and outsourcing (Year 1)
- Product Adoption** → Through free/freemium verification pilots and skilling programs
- Scalable Growth** → Platform-based recurring revenue (Year 2+)
- Ecosystem Build** → Partnerships with government, colleges and industry associations

## Target Customer Segments



### Semiconductor Companies

Design & Verification Teams (India & Global)



### Hardware Startups & MSMEs

Chips, PCB, IoT, Embedded Products



### Engineering Colleges & Universities

VLSI/EDA/PCB Curriculum & Research



### Government & R&D Labs

Semiconductor Mission, ESDM, Pilot Projects



### PCB Design & Electronics Manufacturing

PCB Design Houses, EMS, OEMs



## Go-to-Market Strategy

1



### Build Relationships (Community First)

- Partner with colleges, universities, R&D labs
- Host workshops, hackathons, FDPs, guest lectures
- Create a talent pipeline through internships

2



### Create Value Early (Freemium & Pilots)

- Offer free verification pilots for startups, MSMEs
- Provide limited free access / freemium tier
- Solve real customer problems with quick wins

3



### Engage & Convert (Skilling + Services)

- Train and provide skilled VLSI/PCB resources
- Support startups to adopt AI & automate workflows
- Convert pilot users to paid subscriptions / outsourcing

4



### Scale Through Outsourcing & Platform

- Take up design/verification/PCB projects
- Provide dedicated skilled teams at affordable cost
- Drive platform adoption (SaaS, APIs, enterprise)

5



### Expand via Ecosystem Partnerships

- Collaborate with government (Semiconductor Mission)
- Partner with hardware associations & industry bodies
- Co-develop use cases with OEMs, EMS and design houses

## Customer Journey & Acquisition Funnel



### 1. Awareness

- Workshops, webinars, FDPs
- Thought leadership (LinkedIn, conferences, publications)
- College outreach & industry events

Attract



### 2. Engagement

- Free internships & skilling programs
- Hands-on labs, AI copilot training
- Community (students, startups, engineers)

Engage



### 3. Trial / Pilot

- Free verification pilots
- Freemium platform access
- Solve a real customer use case (quick win)

Build Trust



### 4. Conversion

- Paid platform subscription (₹1,000 – ₹2,000 per user/month (excluding LLM tokens))
- Outsourcing / project contracts
- Hiring skilled resources

Generate Revenue



### 5. Expansion

- Scale usage across departments
- More projects and long-term contracts
- Co-innovation with partners
- Global expansion

Grow Together

## Key Channels



**Colleges & Universities**  
(FDPs, Curriculum, Internships)



**Hardware Startups & MSMEs**  
(Mentoring, Pilots, Affordable Services)



**Government Programs**  
(Semiconductor Mission, ESDM, Grants)



**Industry Associations**  
(IESA, ISBA, PCB & EMS Associations)



**Online & Community**  
(LinkedIn, GitHub, YouTube, Hackathons)

## Value Proposition by Segment

### Students



- Free internships
- AI-powered learning
- Real-world projects
- Career opportunities

### Startups / MSMEs



- Free verification pilots
- Affordable AI tools
- Skilled resources
- Faster time to market

### Enterprises / OEMs



- Cost-effective outsourcing
- Access to skilled teams
- AI-native automation
- Reduced design risk

### Government / Labs



- Alignment with Semiconductor Mission
- R&D collaboration
- Pilot projects
- Talent development

## Pricing Strategy (Very Low Entry Price)



### Platform (SaaS)

₹1,000 – ₹2,000 per user per month (excluding LLM tokens)

- Affordable entry
- Freemium → Paid



### Skilled Resources

- Trained VLSI / Verification / PCB engineers
- Affordable pricing for startups, MSMEs and enterprises
- Flexible engagement models (part-time, full-time)



### Outsourcing / Projects

- Design, verification, PCB review, testbench creation
- End-to-end project support
- Cost-effective and faster turnaround

## Expected Outcomes



Early traction through pilots & skilling programs



Recurring revenue from skilled resources & outsourcing



Platform revenue growth (Year 2+)



Strong ecosystem and long-term partnerships



## 1. Achievements So Far



10+

### Startups Interacted

Understood design, verification and PCB challenges. Strong interest in AI adoption.



20+

### Colleges / Universities

Understood skilling needs in VLSI, PCB, AI, and industry-ready curriculum.



500+

### Students & Faculties Trained

Workshops, FDPs, hands-on sessions across multiple institutions.



### Problem Validation

Confirmed the problem exists: high cost, long cycles, shortage of skilled engineers.



### Strong Interest

Customers are keen to use AI to speed up design/verification and need low-cost tools and skilled resources.

## 2. Product / Technology Development



### Spec-to-RTL Agent

Generate verifiable RTL from natural language

POC Done

MVP in Progress



### Verification Intelligence

Waveform analysis, debug, coverage closure

POC Done

MVP in Progress



### PCB Review Copilot

DFM/DFT/EMI/Thermal predictive analysis

POC Done

MVP in Progress



### AI Tutor (Copilot-Led Lab)

Interactive learning for VLSI, PCB, verification

POC Done

MVP in Progress



### Multi-Agent EDA Kernel

Unified autonomous engineering workflows

Design Phase

Prototype



### Cloud Platform (SaaS + APIs)

Low cost, open-source friendly, scalable

Design Phase

Prototype



### Proof of Concept (POC) for all solutions developed.

MVP development in progress and giving customers early access for testing and feedback.

## 3. Customer / Market Validation



### Startups

10+ startups validated the need for AI-powered design, verification and PCB tools. Keen to pilot and adopt.



### Colleges/ Universities

20+ colleges interested in AI-based skilling programs, curriculum integration and student projects.



### Industry Feedback

Need for skilled VLSI/PCB resources. Looking for low cost tools and AI automation to reduce design time and cost.



### Pilot Opportunities

Multiple opportunities for free verification pilots and training programs. Strong pipeline for paid adoption.

## 4. Roadmap & Key Milestones (Next 24–36 Months)

Q3 2025 – Q1 2026  
(0–6 Months)

### Foundation & Validation

- Complete POC for all core modules
- Engage 20+ colleges and 10+ startups for pilots
- Launch free verification pilots
- Start skilling programs (VLSI & PCB)
- Gather detailed customer feedback

Current Stage

Q2 2026 – Q4 2026  
(6–12 Months)

### MVP Development & Early Adoption

- Release MVP (selected modules)
- Onboard pilot customers (startups, MSMEs, colleges)
- Expand skilling to 500+ students
- Refine product based on user feedback
- Build industry and government partnerships

MVP Launch

2027  
(12–18 Months)

### Market Expansion

- Commercial release (SaaS + APIs)
- Scale skilled resource placement
- Execute paid outsourcing projects
- Expand pilot to enterprise customers
- Build ecosystem with hardware associations and OEMs

Revenue Growth

2028  
(18–24 Months)

### Scale & Diversify

- Full platform with multi-agent workflows
- Growth in SaaS subscriptions
- Increase outsourcing revenue
- Expand to global market opportunities
- Large-scale academic partnerships

Scale Operations

2029+  
(24–36 Months)

### Leadership & Impact

- Become leading AI-native EDA platform in India
- Large customer base across startups, MSMEs and enterprises
- Sustainable revenue from platform, resources and outsourcing
- Contribute to India's Semiconductor Mission

Market Leadership



### Success Metrics

10+

Startups engaged

20+

Colleges/Universities

500+

Students trained

Multiple

Free verification pilots

MVP

In progress

Early Customers

Using the product

Revenue

From resources & outsourcing

Scale to SaaS

Platform revenue (2027+)



## Founder & CEO

Vision • Technology • Innovation



**Dr. Sateesh Ambesange, PhD (AI)**  
IITK (National Institute of Technology Karnataka)



NITK  
PhD (AI)



Stanford  
Ignite / Seed Spark



IIMA  
Business Strategy  
& Communication



SLP Fellow

- **25+ Years** Product Experience | Tech Leadership | Serial Entrepreneur
- Previously worked at **Intel, Philips, Samsung, ST Microelectronics, SanDisk** etc.
- Built several innovative solutions – End to End System Design (Hardware + Software)
- Trained **10,000+** working professionals in AI, GenAI and Agentic AI at **100+** colleges and industry programs
- Mentor, Advisor and Speaker at NITK, IITs, global forums
- Passionate about building an AI-native semiconductor ecosystem for India



PHILIPS

SAMSUNG



life.augmented

SanDisk

## Co-Founder & CTO

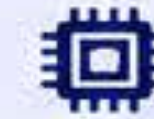
Research • Product • Execution



**Dr. Rashmi Uppin, PhD (AI)**  
M.Tech (VLSI & Embedded Systems)



PhD (AI)  
Research  
& Innovation



M.Tech  
VLSI & Embedded  
Systems



Product  
Development  
& Execution

- 10+ Years of experience in semiconductor, AI and embedded systems
- Leads product architecture, AI models and verification solutions
- Strong research background with focus on AI for EDA and hardware verification
- Drives innovation from POC to MVP to scalable products
- Passionate about skilling students and professionals in VLSI, PCB and AI

“Building AI-native tools and skills to democratize semiconductor design and verification.”  
– Dr. Rashmi Uppin

## Marketing & Partnerships

Growth • Outreach • Ecosystem



**Mallikarjun Patil**  
MBA  
VTU VRIF Mentor



VTU  
VRIF Mentor

- 10+ Years of experience in business development, marketing and strategic partnerships
- Leads customer acquisition, industry collaborations and go-to-market strategy
- Builds relationships with startups, MSMEs, colleges, universities and government programs
- Drives skilling programs, internships and outreach initiatives
- Focused on expanding PragyanAI's ecosystem across India and globally

“Connecting academia, industry and startups for an AI-native semiconductor future.”  
– Mallikarjun Patil



## Advisors & Mentors

- Industry veterans from semiconductor and AI domain
- Mentors from academia and innovation ecosystems
- Guidance on technology, product, go-to-market and strategy



NITK



Stanford  
Ignite / Seed Spark



IIMA



VTU  
VRIF



## Marketing Team

**5+ Senior Professionals**

- Business development
- Industry outreach
- Customer engagement
- Partner ecosystem
- Events, webinars and branding



## Interns & Young Talent

**10+ Interns**

- Students from top engineering colleges
- Work on AI, EDA, verification and tooling
- Gain hands-on industry experience
- Contribute to product development, research and customer projects



## College Collaboration & Faculty Network

**20+ Colleges / Universities**

- Curriculum collaboration in VLSI, PCB and AI
- Internships, training programs and FDPs
- Joint research and student projects
- Faculty engagement and knowledge exchange
- Building the next generation of skilled engineers



**Our Collective  
Strength**



**25+**  
Years Industry  
Experience



**10K+**  
Professionals  
Trained



**100+**  
Colleges & Institutions  
Engaged



**10+**  
Startups  
Interacted



**Multiple**  
Innovative  
Solutions Built



**Strong**  
Industry &  
Academic Network



## 1 Mentorship & Expert Guidance

- |  |                              |                                                                                                                                                                                                                                                       |
|--|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Technology Guidance</b>   | <ul style="list-style-type: none"> <li>Connect with domain experts and faculty members</li> <li>Collaborate with faculties to develop advanced AI/EDA solutions</li> <li>Guidance on semiconductor design, verification and AI integration</li> </ul> |
|  | <b>Business Strategy</b>     | <ul style="list-style-type: none"> <li>Go-to-market strategy, market positioning</li> <li>Pricing, revenue model and scaling plan</li> <li>International market expansion guidance</li> </ul>                                                         |
|  | <b>Product Development</b>   | <ul style="list-style-type: none"> <li>Product roadmapping and prioritization</li> <li>User validation and feedback</li> <li>Best practices for building scalable products</li> </ul>                                                                 |
|  | <b>IP / Legal</b>            | <ul style="list-style-type: none"> <li>IP filing strategy (patents, trademarks, copyrights)</li> <li>Legal support for collaborations and licensing</li> <li>Guidance on open-source and proprietary models</li> </ul>                                |
|  | <b>Fundraising Readiness</b> | <ul style="list-style-type: none"> <li>Investor pitch deck review</li> <li>Financial modeling and unit economics</li> <li>Introduction to early-stage investors and grants</li> </ul>                                                                 |



## 2 Infrastructure & Facilities

- |  |                                             |                                                                                                                                                                                                                                                 |
|--|---------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Office / Co-working Space</b>            | <ul style="list-style-type: none"> <li>Dedicated workspace for core team</li> <li>Meeting rooms and collaboration space</li> <li>Access to incubation community</li> </ul>                                                                      |
|  | <b>Lab / Technical Infrastructure</b>       | <ul style="list-style-type: none"> <li>High-performance computing (GPU servers)</li> <li>EDA tools and hardware design software access</li> <li>Secure cloud / on-prem infrastructure</li> </ul>                                                |
|  | <b>Testing &amp; Prototyping Facilities</b> | <ul style="list-style-type: none"> <li>Access to semiconductor design &amp; verification test infrastructure</li> <li>PCB prototyping and hardware testing facilities</li> <li>Support for real hardware validation and measurements</li> </ul> |

## 3 Market & Industry Access

- |  |                                         |                                                                                                                                                                                                                                        |
|--|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Corporate / Industry Connections</b> | <ul style="list-style-type: none"> <li>Introductions to semiconductor, electronics and hardware manufacturing companies</li> <li>Access to industry experts and technical champions</li> </ul>                                         |
|  | <b>Customer Discovery</b>               | <ul style="list-style-type: none"> <li>Facilitate interactions with startups, MSMEs and enterprises</li> <li>Support in pilot discussions and customer validation</li> <li>Feedback from industry on product roadmap</li> </ul>        |
|  | <b>Pilot Opportunities</b>              | <ul style="list-style-type: none"> <li>Help secure pilot projects with industry and government</li> <li>Connect with real-world use cases</li> <li>Facilitate long-term engagements and contracts</li> </ul>                           |
|  | <b>Strategic Partnerships</b>           | <ul style="list-style-type: none"> <li>Partnerships with EDA companies, OEMs, fabs, design houses</li> <li>Collaboration with academic and research institutions</li> <li>Joint development and co-innovation opportunities</li> </ul> |

## 4 Startup Ecosystem Support

- |  |                                       |                                                                                                                                                                                                                                                |
|--|---------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Networking</b>                     | <ul style="list-style-type: none"> <li>Access to startup community and alumni network</li> <li>Connect with successful deep-tech entrepreneurs</li> <li>Peer learning and collaboration opportunities</li> </ul>                               |
|  | <b>Investor Connect</b>               | <ul style="list-style-type: none"> <li>Introductions to seed and early-stage investors</li> <li>Venture capital and strategic investors</li> <li>Participation in investor meets and demo days</li> </ul>                                      |
|  | <b>Government / Ecosystem Connect</b> | <ul style="list-style-type: none"> <li>Support in applying for government grants and schemes (MeitY, DST, etc.)</li> <li>Connect with semiconductor mission initiatives</li> <li>Linkages with policy makers and public sector labs</li> </ul> |
|  | <b>Events &amp; Showcases</b>         | <ul style="list-style-type: none"> <li>Opportunity to present at ORBIT events</li> <li>Participation in technology showcases, exhibitions</li> <li>Access to national and international conferences</li> </ul>                                 |

## 5 Other Specific Support Required

- |  |                                    |                                                                                                                                                                                                                                 |
|--|------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Talent Support</b>              | <ul style="list-style-type: none"> <li>Help in hiring skilled research and engineering talent</li> <li>Intern support through college network</li> <li>Access to talent pool and fellowship programs</li> </ul>                 |
|  | <b>Academic Collaboration</b>      | <ul style="list-style-type: none"> <li>Facilitate collaboration with NITK and other institutes</li> <li>Joint research projects and student internships</li> <li>Access to faculty expertise in AI, VLSI and EDA</li> </ul>     |
|  | <b>International Exposure</b>      | <ul style="list-style-type: none"> <li>Support for global partnerships and market access</li> <li>Participation in international programs and delegations</li> <li>Guidance on global standards and compliance</li> </ul>       |
|  | <b>Business Operations Support</b> | <ul style="list-style-type: none"> <li>Guidance on company structure, compliance and governance</li> <li>Support for HR, finance, and operational processes</li> <li>Access to domain experts for scaling operations</li> </ul> |



## Elevator Pitch

We are building an affordable, **AI-native platform and services** to democratize **semiconductor design and verification**, powered by LLMs, domain expertise and hands-on skilling — from design to deployment.



Faster Design & Verification



Lower Cost & Higher Productivity



Skilled Talent for a Stronger India Semiconductor Ecosystem

From Design to Deployment with AI



## Key Differentiators / USP

A Complete, Affordable and Integrated Solution for Semiconductor Design, Verification & Skilling

### 1 Balanced Business Model (Services + Product)



#### Services (Immediate Revenue)

- Skilled resources
- Training & consulting
- Solution outsourcing



#### Products (Scalable Growth)

- AI-native EDA tools
- Verification intelligence
- Autonomous workflows

Sustainable revenue to fund and accelerate product development

### 2 Domain-Specific AI with LLM Fine-Tuning



#### Domain Fine-Tuned LLM for Semiconductor

- Fine-tuned on semiconductor/EDA domain (specs, RTL, UVM, DFT, manufacturing, failure data)
- Higher accuracy and relevance than general-purpose LLMs
- Retrieval-Augmented Generation (RAG) with hardware knowledge graphs
- Continuously improves from user data and verification cycles

Specs & Standards

RTL / UVM

Verification Logs

Manufacturing Data

Knowledge Graphs

### 3 End-to-End Comprehensive Solution (Integrates with Existing Tools)

Design

Verify

Debug

Optimize

Deploy

- Complete workflow: spec → design → verification → debug → sign-off → manufacturing
- Integrates with industry tools (Cadence, Synopsys, Siemens, Ansys, etc.)
- Adds AI layer without disrupting existing workflows
- Unified platform with multi-agent automation, knowledge graphs and analytics
- Modular deployment — adopt step-by-step or full-stack

### 4 Affordable & Accessible



- Significantly lower cost than legacy tools
- Freemium verification pilot for easy adoption
- Subscription-based platform (₹1K–2K/month + LLM token cost)
- Affordable for startups, MSMEs, colleges and R&D teams



Low Entry Cost



Freemium Pilot



Inclusive Pricing for Academia & Startups

### 5 Skilling + Ecosystem Enablement



- Trains next generation engineers in VLSI, PCB and AI
- Provides skilled resources to industry at affordable cost
- Collaborates with colleges, government and industry associations
- Builds an AI-ready semiconductor workforce ecosystem



Colleges & Universities



Government Programs



Industry Associations



Internships & Mentorship

### 6 Proprietary & Continuously Learning Data Moat



- Every verification run, debug cycle and user interaction generates valuable data
- Includes defect patterns, EMI/thermal risks, manufacturing insights and debugging graphs
- Data improves models, tools and recommendations over time
- Builds the largest AI-native hardware failure & verification intelligence system



Unique Dataset



Better AI Accuracy



Increasing Value Over Time

### 7 Expert Founding Team with Rare Combination



- 25+ years industry experience in VLSI, embedded systems and product engineering
- Strong AI expertise with PhD and research background
- Proven track record in building innovative solutions and businesses
- Committed, passionate and execution-focused team

Experience + Domain Knowledge + AI + PhD + Serial Entrepreneurship

### 8 Open & Extensible Ecosystem



- Leverages and integrates with open-source EDA infrastructure (e.g., KiCad, Verilator, OpenROAD, Yosys)
- Open APIs and modular architecture
- Enables collaboration with startups, academia and industry
- Supports custom extensions and domain-specific use cases

</> Open APIs



Modular Architecture



Ecosystem Collaboration

### 9 Real-World Impact & India Focus



- Democratize access to advanced semiconductor tools
- Accelerate innovation for startups, MSMEs and academia
- Build a self-reliant and skilled semiconductor ecosystem for India and the world
- Enable faster, cost-effective and high-quality chip design and verification

Stronger India Semiconductor Ecosystem



The PragyanAI Advantage



Domain-Focused AI (not generic)



Affordable & Accessible



End-to-End Integration



Service + Product for Sustainable Revenue



Skilling & Ecosystem



Scalable Global Impact

<https://pragyanai-pcb-varification-solutions-poc.streamlit.app/>

[https://github.com/pragyanaischool/PragyanAI\\_PCB\\_Verification\\_Solution](https://github.com/pragyanaischool/PragyanAI_PCB_Verification_Solution) Share ☆ ✎ 🔄 ⋮

App Settings

Analysis Mode

Full (Accurate) ▼

- ☒ Show Raw Outputs
- ☒ Cleanup temp files

i Info

- Multi-Agent AI
- Power / Signal / Thermal / Layout
- Vision + OCR + Graph + GNN

PragyanAI PCB Copilot



Grow with Gyan

Multi-Agent AI for PCB Analysis (Vision + Graph + LLM + GNN)

Upload PCB Image or Netlist

 buggy\_amp.txt × +  
353.0B

Supported Inputs

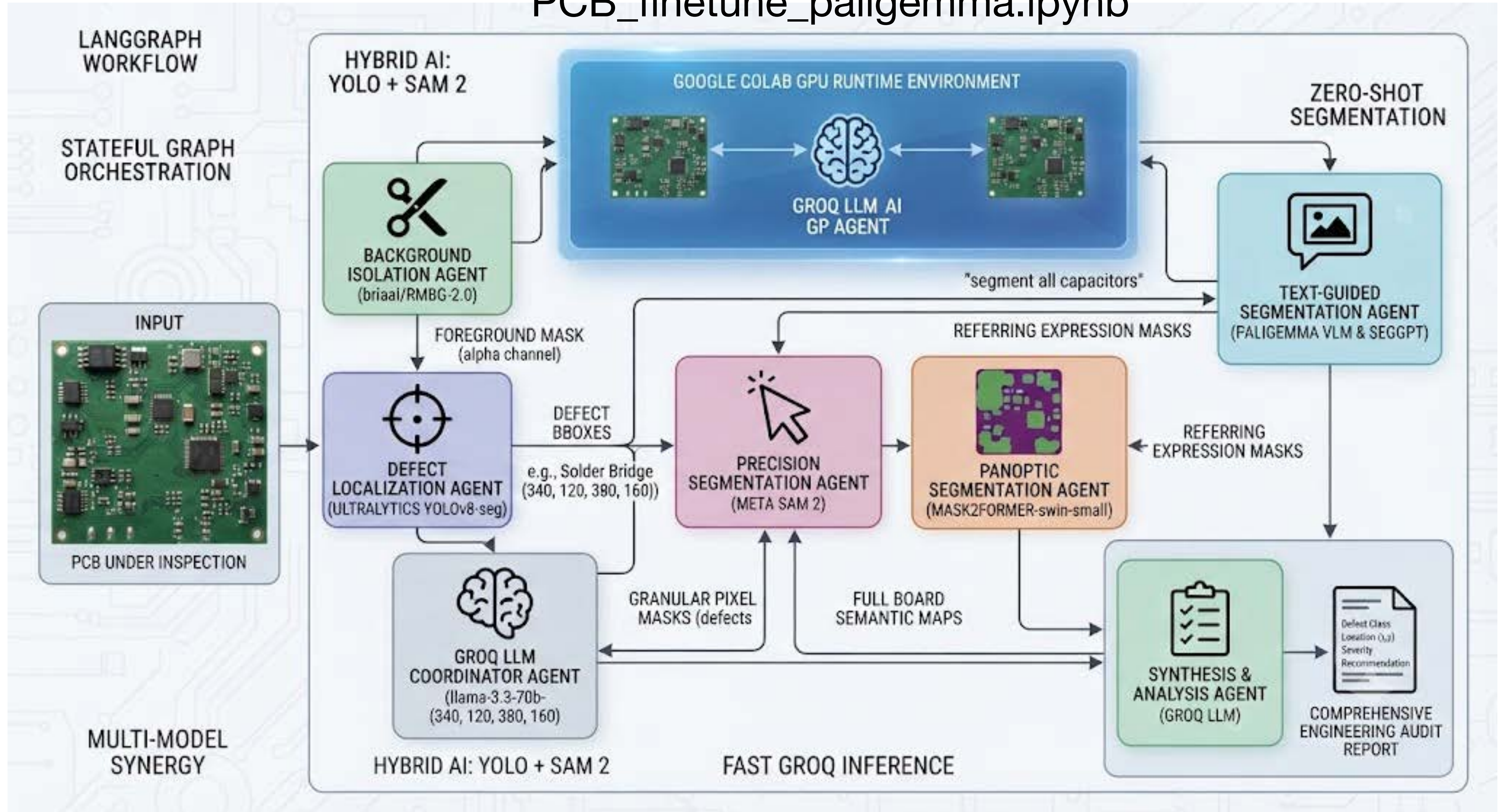
- PCB Images
- Netlist Files

Run AI Analysis

Analysis Completed

# PCB\_Related Projects.ipynb

## PCB\_finetune\_paligemma.ipynb



# PCB\_Related Projects.ipynb

<https://github.com/pragyanaischool/PragyanAI-PCB-Varifications-Solutions>

### Settings

Analysis Mode

Full (Accurate) ▾

☒ Show Debug Info

### PCB Verification Stack

- Vision Defect Localization
- IPC-A-610 Rule Checking
- Topological Graph Engine
- Multi-Agent Orchestration

### Chat Controls

Clear Chat

Reset Memory

Show Memory

Share ☆ ✎ ↺ ⋮

## PRAGYAN AI

Grow with Gyan

# PragyanAI PCB Copilot

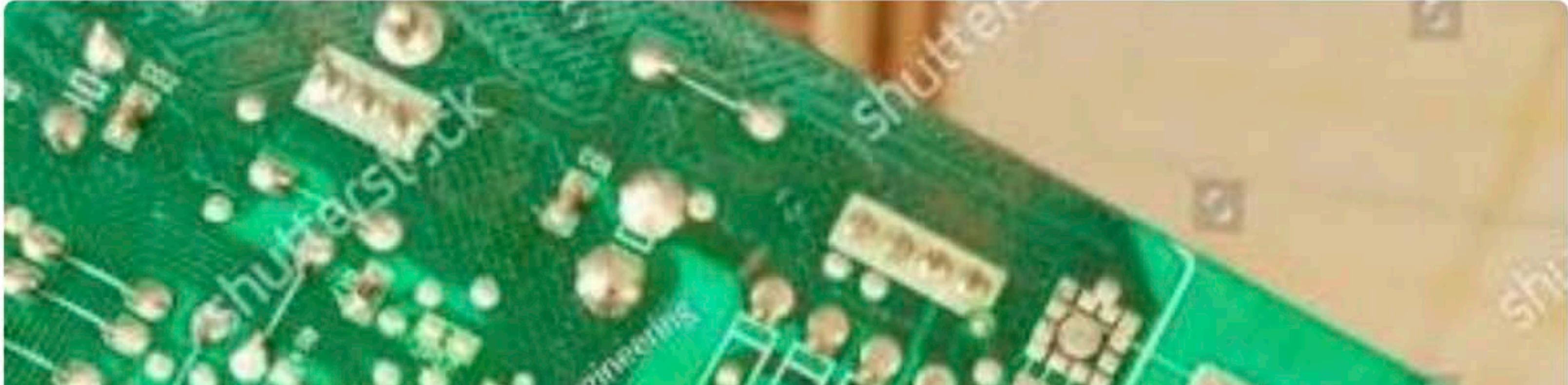
Vision + YOLO + Segmentation + Multi-Agent AI + RAG

Upload PCB Image

 PCB\_damaged.jpeg 47.0KB +

Upload Datasheet / Spec PDF (Optional)

 Upload 200MB per file • PDF



# PCB\_Related Projects.ipynb

<https://github.com/pragyanaishchool/PragyanAI-PCB-Verifications-Solutions>

### Settings

Analysis Mode

Full (Accurate) ▾

☒ Show Debug Info

---

### PCB Verification Stack

- Vision Defect Localization
- IPC-A-610 Rule Checking
- Topological Graph Engine
- Multi-Agent Orchestration

### Chat Controls

Clear Chat

Reset Memory

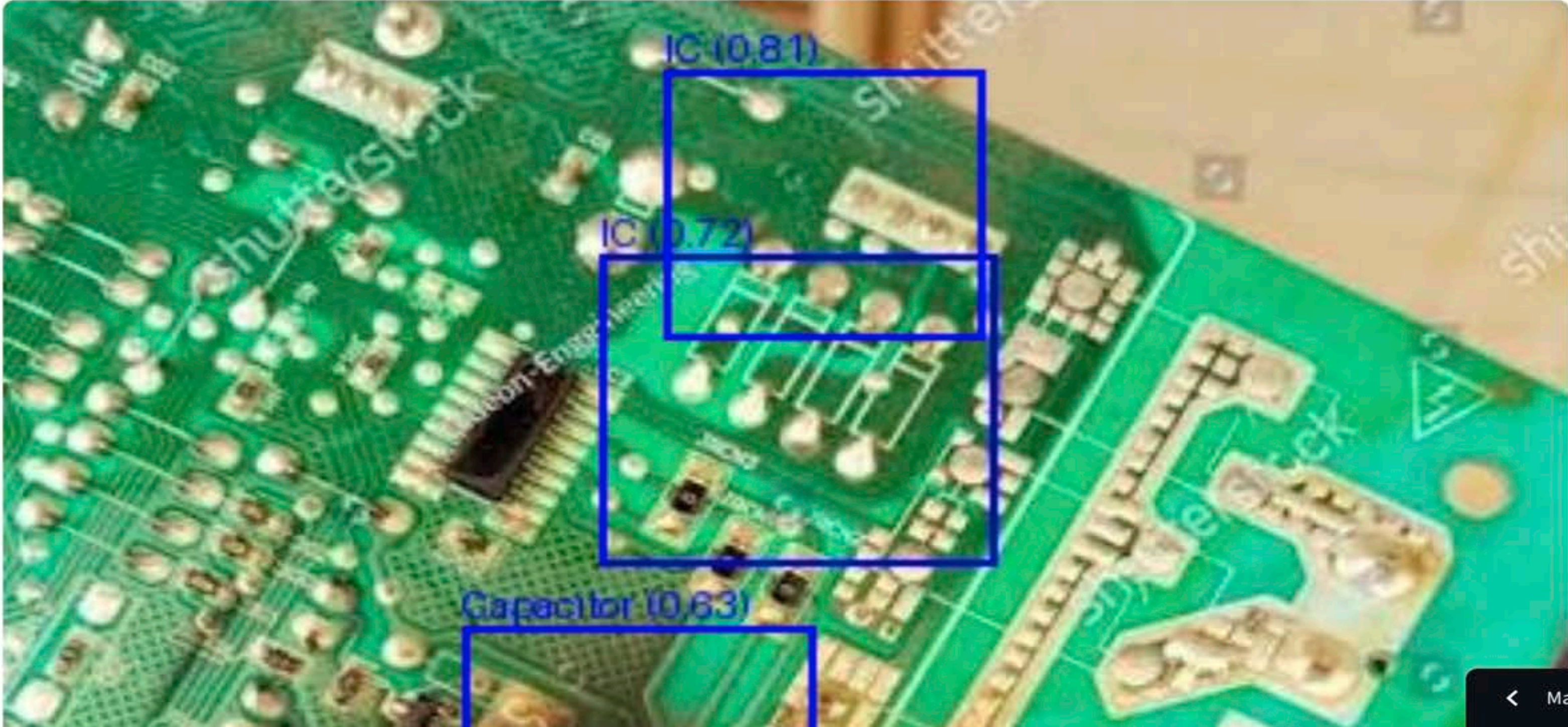
Show Memory

Share ☆ ✎ ↺ ⋮

1. Final Report 2. Visualization 3. Vision AI 4. Insights 5. Domain Rules 6. Graph Summary 7. Debug 8. Chat AI

## PragyanAI PCB Visualization

☒ Show Components☒ Show Issues☒ Show Heatmap



< Manage app

<https://pragyanai-pcb-part1-planning-engine-solution-ah7xd8irnzed5wkym.streamlit.app/>

<https://github.com/pragyanaishchool/PragyanAI-PCB-Part1-Planning-Engine-solution>



Grow with Gyan

Planning Engine

LLM: openai/gpt-oss-120b (Groq)

State Machine: LangGraph

Embeddings: HF all-mpnet-base-v2

Reset Session

Share ☆ ✎ ↺ ⋮



# Grow with Gyan

## PragyanAI Element 1: Planning & Strategy

Transform natural language PRDs into validated `architecture_plan.json` files.

### Input: Product Requirements (PRD)

Describe your hardware project in detail:

A solar-powered IoT weather station with BME280 sensor, ESP32-S3, and an e-paper display. Must operate at 3.3V.

### Output: Architecture Plan

```
{
  "mcu": {
    "family": "ESP32-S3"
    "package": "ESP32-S3-WROOM-1"
  },
  "power_tree": [
```

<https://pragyanai-frontenddesignspecification.streamlit.app/>

[https://github.com/pragyanaischool/pragyanai\\_eda\\_aiagentic\\_vlsi-front-end-design-specifications\\_sol/](https://github.com/pragyanaischool/pragyanai_eda_aiagentic_vlsi-front-end-design-specifications_sol/)

<<

app

Knowledge Base

Spec Designer

Spec Chat

RTL Generator

Verification Bench

PRAGYAN AI

Grow with Gyan

Share ☆ ↗ ↻ ⋮

PRAGYAN AI

Grow with Gyan

# PragyanAI: Multi-Agent VLSI Design Suite

## Autonomous Chip Design Framework with RAG, RTL Gen & HITL

Welcome to **MAGE** (Multi-Agent General Engine) tailored for VLSI Front-End Design. This platform automates the entire lifecycle—from **RTL Design Specifications (RDS)** to **Synthesizable Code** and **Self-Checking Testbenches**—by leveraging specialized AI agents and your local technical library.

👉 Select a page from the sidebar to begin your design journey.

<https://pragyanai-frontenddesignspecification.streamlit.app/>

[https://github.com/pragyanaishool/pragyanai\\_eda\\_aiagentic\\_vlsi-front-end-design-specifications\\_sol/](https://github.com/pragyanaishool/pragyanai_eda_aiagentic_vlsi-front-end-design-specifications_sol/)



## 1. Knowledge Base

Upload your PDF standards (AXI, PCIe, RISC-V, etc.). The **RAG Engine** indexes these locally using HuggingFace embeddings for precise technical grounding.

## 2. Spec Designer

Enter a problem statement. The **Architect** drafts the RDS, the **Critic** audits for CDC/Protocol errors, and you provide **Human-in-the-Loop** refinements to create the "Golden Spec".

## 3. Spec Chat

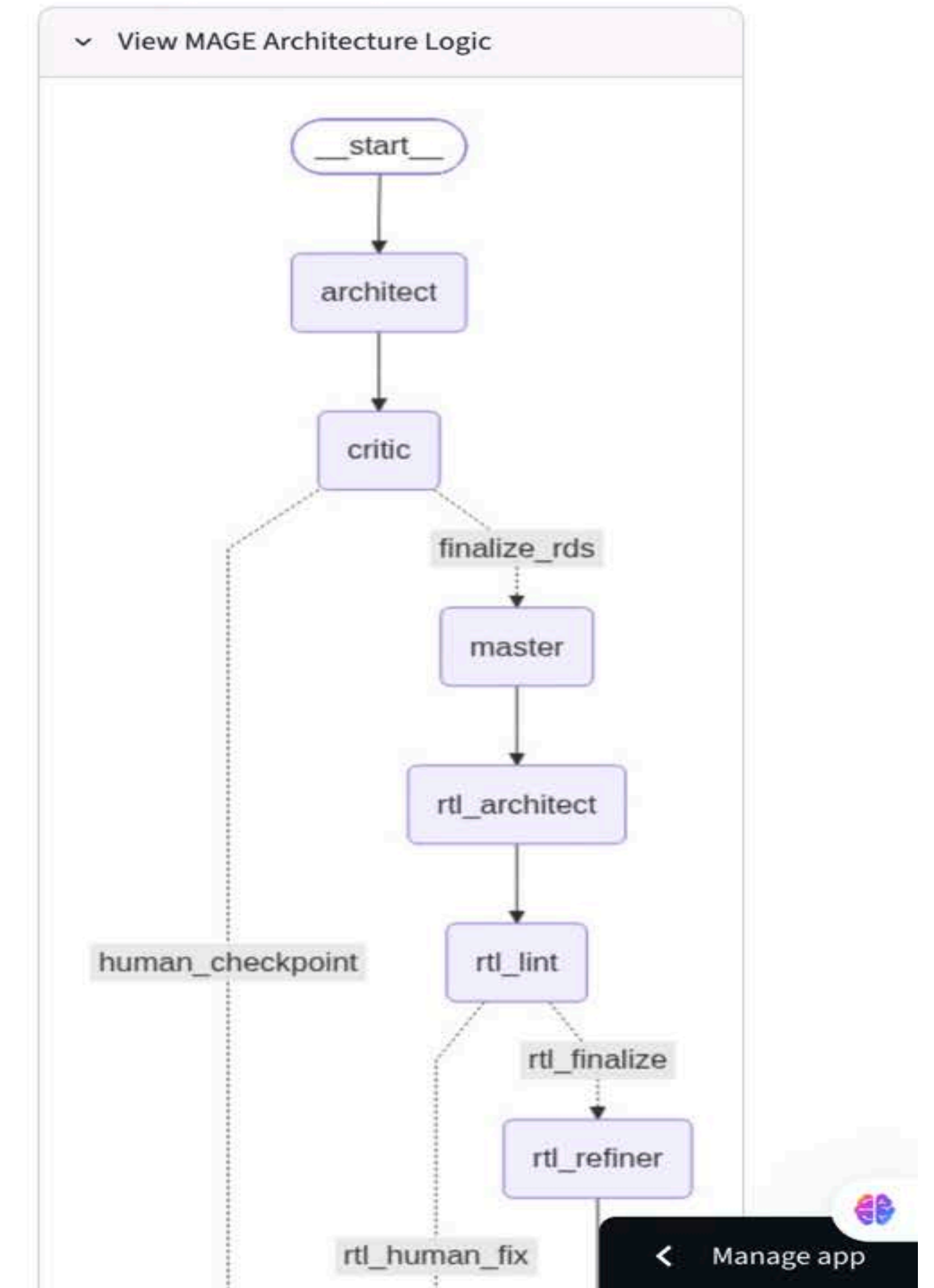
Interact with your generated specification. Ask questions about design choices or protocol nuances found in your uploaded documents.

## 4. RTL Generator

Translate your RDS into production-ready **Verilog** or **VHDL**. Includes an automated **Linting Agent** to catch "design killer" bugs like unintentional latches.

## 5. Verification Bench

Generate a **Self-Checking Testbench**. This phase includes a **DV Lead Agent** that explains the rationale behind every test case (Corner cases, Reset, and Stress tests).



<https://pragyanai-frontenddesignspecification.streamlit.app/>

[https://github.com/pragyanaischool/pragyanai\\_eda\\_aiagent\\_vlsi-front-end-design-specifications\\_sol/](https://github.com/pragyanaischool/pragyanai_eda_aiagent_vlsi-front-end-design-specifications_sol/)

app

Knowledge Base

Spec Designer

Spec Chat

RTL Generator

Verification Bench

# RTL Design Specification (RDS) – 32-Bit Pipelined Adder

Document Revision: 1.0 – 2026-09-25  
Author: Principal VLSI Architect

## 1. Functional Overview

| Item                    | Description                                                                                                                                                                                                                                                                                                                                                |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Block name              | adder32_pipe                                                                                                                                                                                                                                                                                                                                               |
| Purpose                 | Provide a high-throughput, fully synchronous 32-bit unsigned (or two’s-complement) addition service to the SoC. The block is deliberately pipelined to achieve one-addition-per-clock-cycle throughput after pipeline fill, while keeping the combinational delay of the adder itself well within a single clock period.                                   |
| SoC integration context | The adder is a shared arithmetic accelerator used by multiple masters (e.g., CPU, DMA, DSP). It is accessed through a memory-mapped register interface on the APB/AXI-Lite bus. The design follows the standard <b>Peripheral Register Interface (PRI)</b> used across the SoC, enabling easy inclusion in the address decoder and power-management block. |

# Technical Audit – RTL Design Specification (RDS) “32-Bit Pipelined Adder”

Document Reviewed: RDS Draft v1.0 (2026-09-25)  
Auditor: Senior DV Engineer  
Date: 2026-09-25

## 1. Executive Summary

The specification describes a clean, two-stage, fully-synchronous 32-bit adder intended for APB/AXI-Lite access. The high-level architecture is sound, but several **design-killer** risks are either implicit or omitted:

| Area                             | Severity | Comments |
|----------------------------------|----------|----------|
| <div><div>Manage app</div></div> |          |          |

<https://pragyanai-siliconai-ip-dataset-rag-assistant.streamlit.app/>

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# Grow with Gyan

## IP Core & Knowledge Base Management (SQL + FAISS CPU)

Organize semiconductor IPs stored persistently in SQLite database, manage added documents, ingest multi-source data into FAISS CPU Vector Store, and retain information across sessions.

### 1. Select Existing Group / Protocol Family or Create New

Protocol Group Management

Select Existing Group ▼

IP Model / Version Identifier

e.g., PCIe\_Gen2, AXI4\_Interconnect

IP Group / Protocol Family

e.g., PCIe, AMBA, SPI, RISCv

Register / Set Active IP Container



### PragyanAI Silicon RAG

Hardware IP & Datasheet Engineering Suite

#### Navigation Menu

- ☒ Ingestion & IP Management
- ☐ Interactive IP RAG Chat
- ☐ References & Citation Dashboard
- ☐ Spec & Version Comparison
- ☐ Document Viewer & Page Summarizer

#### Registered IP Families

No IP models registered yet. Go to Ingestion to start.

< Manage app

<https://g2tuiszyrge4wvg2ky9bgz.streamlit.app/>

[https://github.com/pragyanaischool/PragyanAI\\_EDA\\_PCB\\_Part2\\_Implementation\\_Core\\_Solutions/](https://github.com/pragyanaischool/PragyanAI_EDA_PCB_Part2_Implementation_Core_Solutions/)

app

Blueprint

Synthesis

Intelligence

Visualizer

PRAGYAN AI

Grow with Gyan

PragyanAI Studio

Select Workspace:

☒ Phase 1: Architecture & Critic

☐ Phase 2: PCB EDA & Defect Prediction

Phase 1: Architecture & RAG Critic

Establish the logical foundation and validate via AI Reviewer.

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PRAGYAN AI

Grow with Gyan

Phase 1: AI Architect & Critic

Welcome to the **PragyanAI Implementation Core**. This phase facilitates the **Human-in-the-Loop** transition from planning to synthesis. Review your Architecture Plan, run the **RAG Critic**, and finalize the logic before generating engineering artifacts.

Project Name

e.g., Smart AgTech Sensor Hub V2

Upload Architecture JSON

Upload

200MB per file • JSON

Manage app

https://g2tuiszyrge4wvg2ky9bgz.streamlit.app/

https://github.com/pragyanaischool/PragyanAI\_EDA\_PCB\_Part2\_Implementation\_Core\_Solutions/

Grow with Gyan

PragyanAI Studio

Select Workspace:

Phase 1: Architecture & Critic

Phase 2: PCB EDA & Defect Prediction

Phase 2: Core Solutions EDA

Analyze production line telemetry and evaluate real-time defect risk.

Upload Inspection Data (CSV)

Upload

200MB per file • CSV

Agentic Pipeline Status:

Architect Agent: Online

Critic Agent: RAG-Enabled

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PRAGYAN AI

Grow with Gyan

PCB Inspection & Defect Risk Analytics

Automated exploratory telemetry analysis and predictive defect assessment.

Total Inspected Boards

Defect Rate

Defective Units

Mean Reflow Temp

1,500

20.80%

312

244.7 °C

↑ 5.8% vs baseline

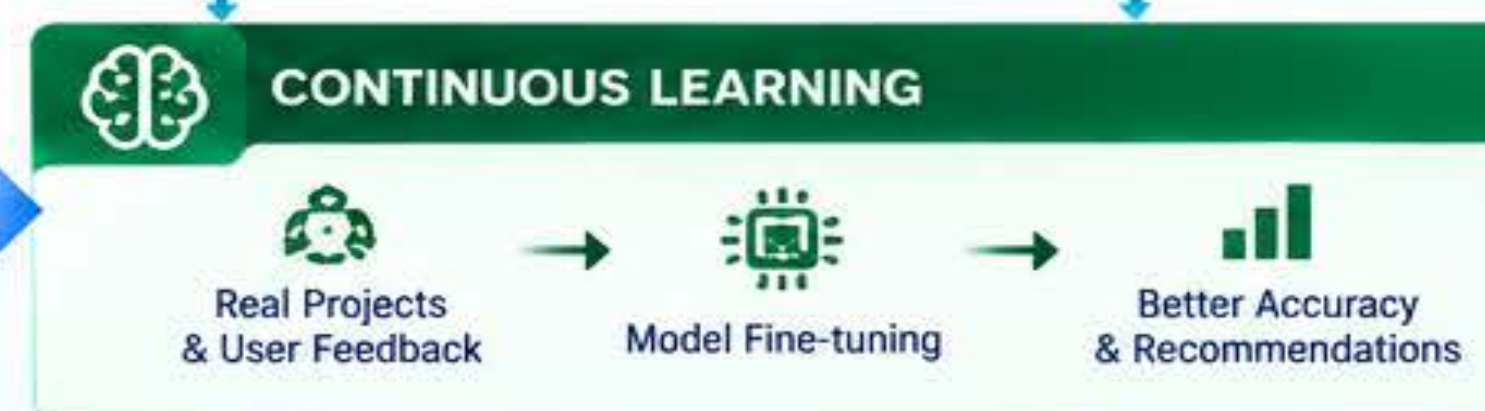
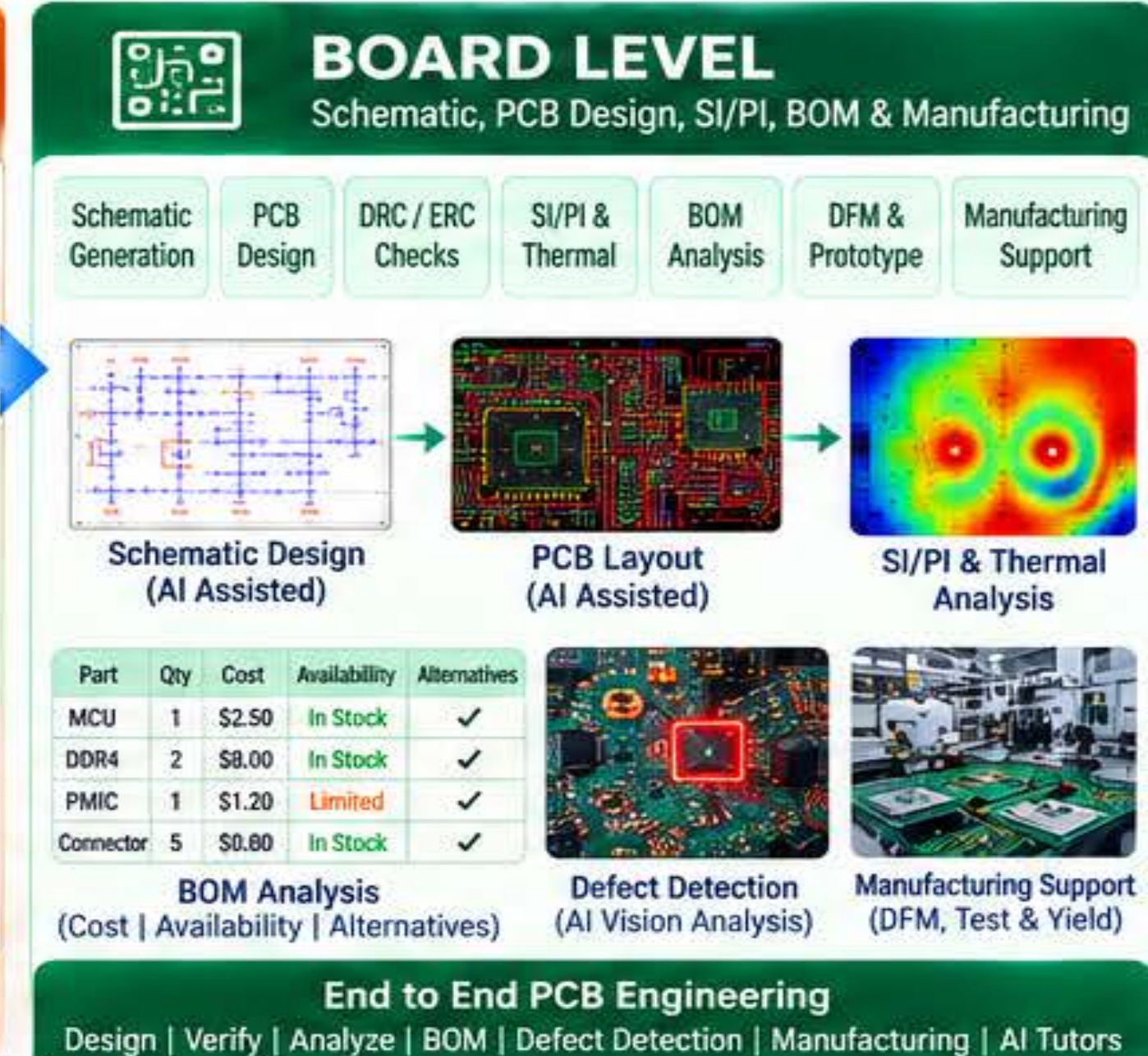
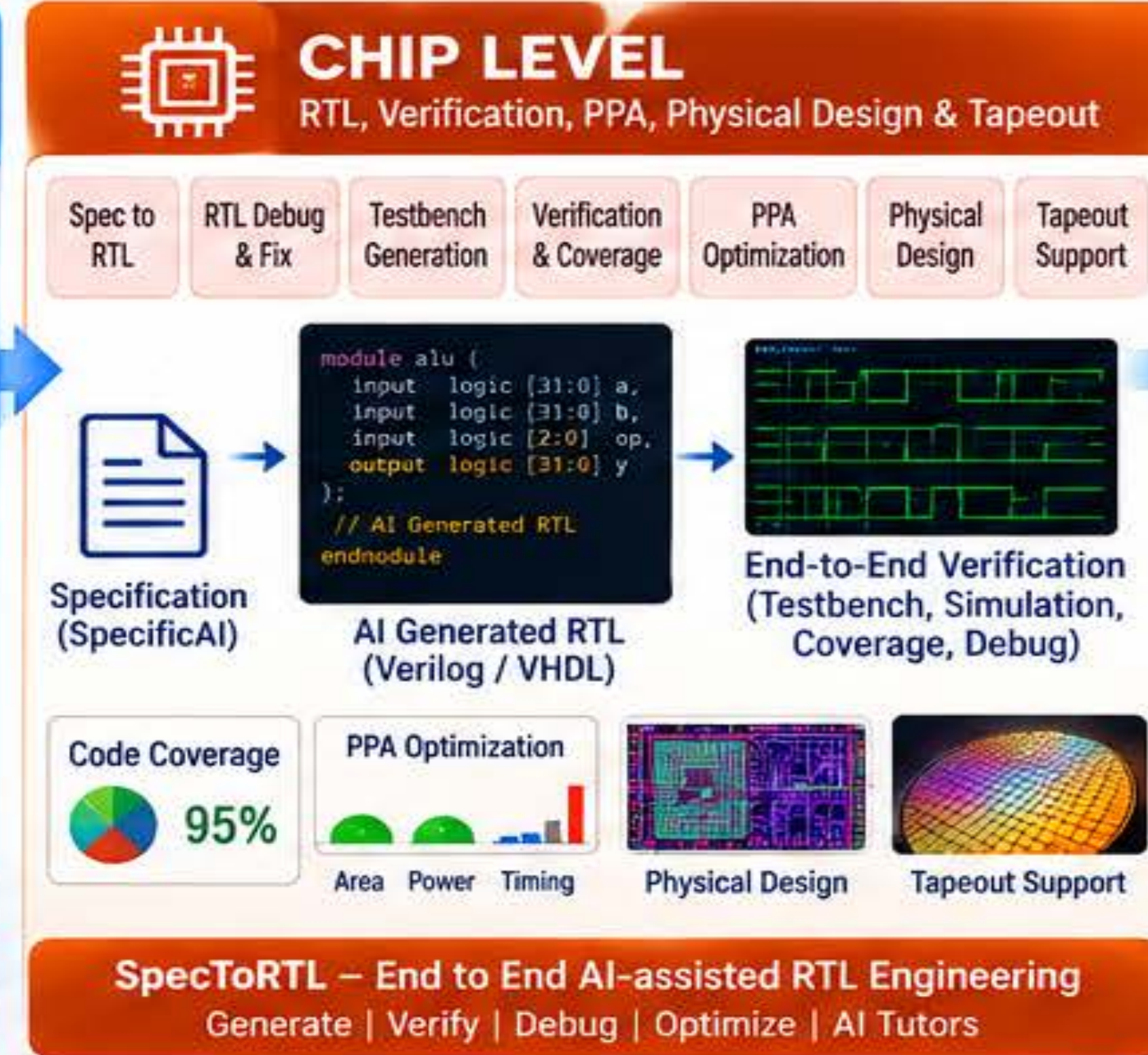
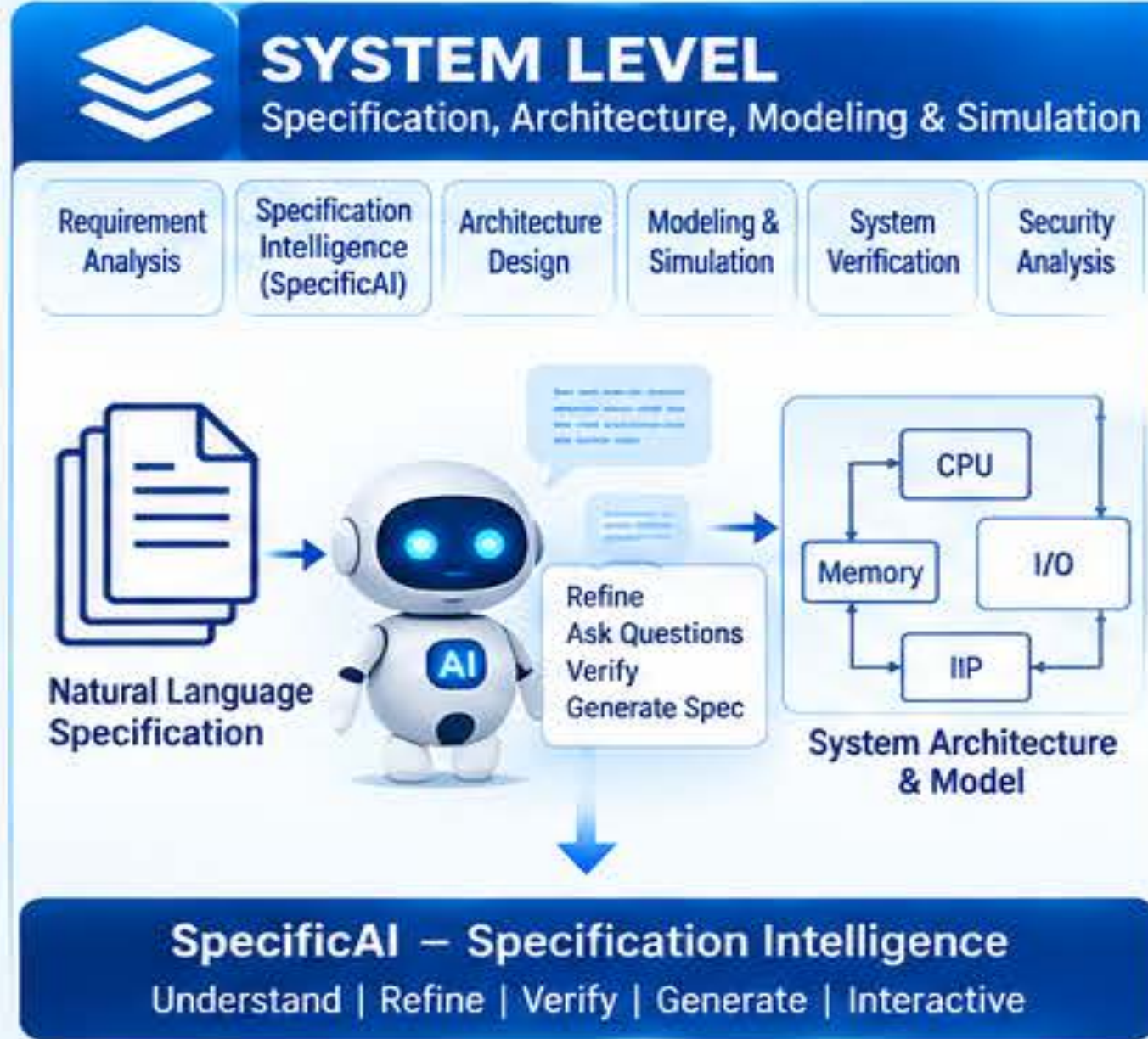
Interactive EDA

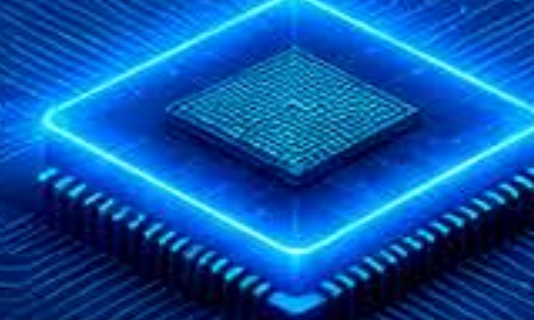
Model Diagnostic

Live Defect Predictor

Process Telemetry vs. Defect Rate

Manage app





## 1 Our Vision



“To become the leading **AI-native platform** for **semiconductor design, verification and skilling**, powering the next generation of chips and talent for India and the world.”

## 2 Key Business & Technology Goals

- Build Scalable AI Platforms**  
Complete MVPs and launch core products (verification, copilots, multi-agent EDA).
- Create Revenue Streams**  
Platform subscriptions, skilled resources and solution outsourcing.
- Gain Customer Traction**  
Convert pilots to paid customers (startups, MSMEs, OEMs, academia).
- Build Talent Pipeline**  
Train 10,000+ engineers in VLSI, PCB and AI tools.
- Establish Partnerships**  
Collaborate with industry, government, colleges and global ecosystem players.

## 3 Expected Scale (By 24 Months)

- 10,000+ Engineers Trained**  
(students & working professionals)
- 100+ Colleges / Universities**  
Partnered
- 50+ Startups & MSMEs**  
Using Our Platform
- 10+ Industry / OEM Engagements**
- ₹1–2 Cr Annual Revenue**  
(run-rate, from platform + services)
- 3–5 Flagship Customers**  
with long-term contracts

## 4 12–24 Month Growth Plan (Roadmap)



## 5 Expansion Plans

- 
- Pan-India expansion across colleges, startups and industry clusters
  - Expand to SEA, US and Europe (through academic and industry partnerships)
  - Add more domain-specific tools (PCB, packaging, system design)
  - Build a global community of skilled engineers

## 6 Long-term Impact

- Accelerate Semiconductor Innovation**
- Create Skilled Workforce at Scale**
- Enable Atmanirbhar Bharat in Chips**
- Global Leadership in AI-native EDA Solutions**

## 7 Why Orbit / Why IIITB Innovation Centre?

- 
- Access to world-class mentors and domain experts
  - Research collaboration with IIITB faculty and labs
  - State-of-the-art infrastructure and incubation ecosystem
  - Industry, investor and government connect
  - Credibility, visibility and faster go-to-market

### 1 Deep Industry Experience in VLSI & Embedded Systems

- Founders have 25+ years of hands-on experience in semiconductor, VLSI, embedded systems and product engineering.
- Previously worked at **Intel, Philips, Samsung, STMicroelectronics, SanDisk** and other global companies.
- End-to-end experience from architecture to silicon and product development.



PHILIPS

SAMSUNG



SanDisk



### 2 Strong AI Expertise & Academic Depth (PhD)

- Founders have PhD in AI and strong research background.
- Deep expertise in AI, GenAI, Agentic AI, LLMs and applying AI to EDA and hardware.
- Built and trained 10,000+ professionals in AI, GenAI and Agentic AI at 100+ colleges and industry programs.
- Active research, publications, and collaboration with academic institutions.



### 3 Proven Track Record in Establishing Businesses

- Experience in building and scaling products and services.
- Understanding of market, customers, pricing and go-to-market strategies.
- Strong industry and academic network across India and global ecosystem.
- Experience in partnerships, collaborations and program execution.



### 4 Balanced Service + Product Model

- Offer skilled resources, training, consulting and outsourcing services to generate early and sustainable revenue.
- Use the revenue to fund and accelerate our AI-native product development.
- Provides financial stability, customer access and real-world feedback for rapid product innovation.



✓ Stable Revenue    ✓ Faster Product Development    ✓ Sustainable Growth



### 5 Committed, Passionate & Proven Perseverance

- Consistent execution over many years across training, product development and industry collaborations.
- Engaged with 10+ startups and 20+ colleges to validate the problem and solution.
- Built POCs, MVPs and working prototypes across multiple solutions.
- Strong commitment to create impact through skilling, innovation and industry adoption.



### 6 A Rare Combination That Wins



VLSI + Embedded  
Domain Expertise

Real industry experience  
from architecture to silicon



AI Expertise  
& PhD

Deep research and  
applied AI knowledge



Business  
Building Experience

Product, market,  
revenue and scaling



Balanced  
Service + Product

Sustainable revenue  
to enable product growth



Commitment &  
Perseverance

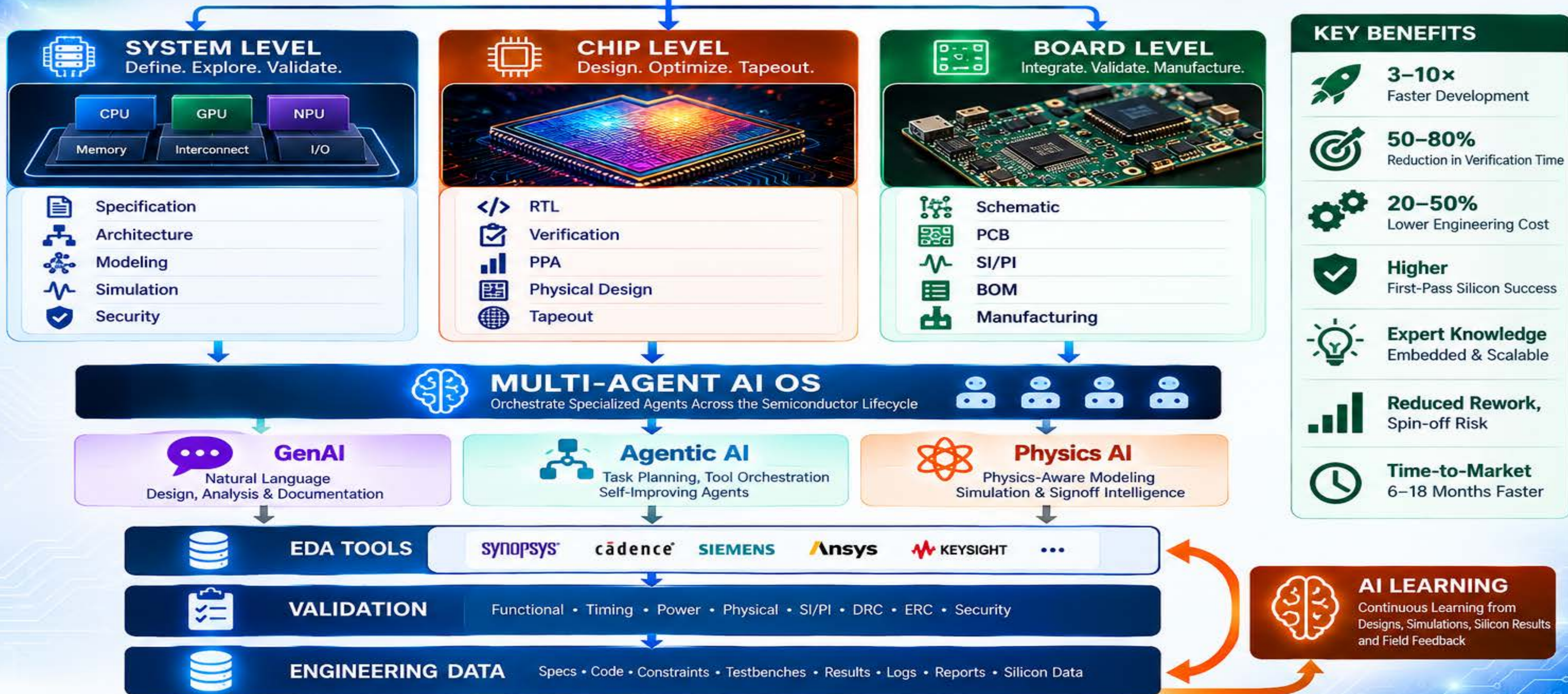
Proven execution and  
long-term vision



**A Stronger, More Capable  
and Impact-Driven Team**

Few teams bring together  
this unique blend of industry experience,  
domain knowledge, AI expertise, PhD and  
serial entrepreneurship.

This unique combination positions PragyanAI to build an **AI-native, accessible and world-class semiconductor ecosystem** for India and the world.

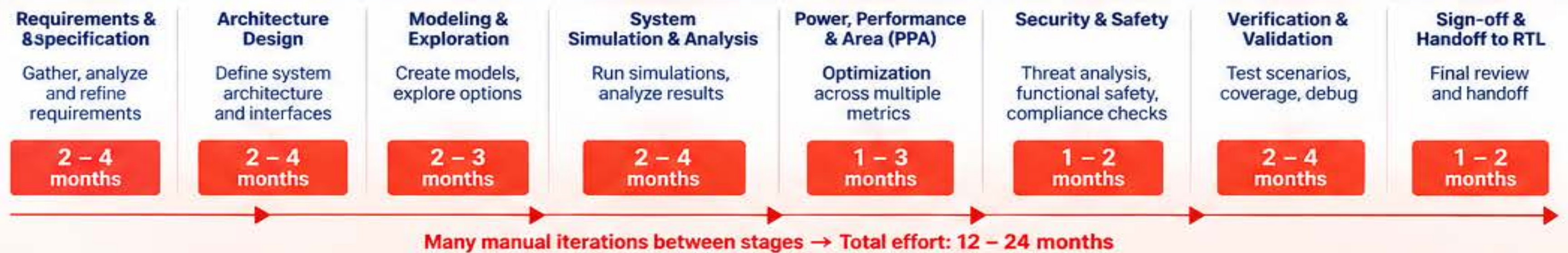


### SYSTEM LEVEL TASKS IN SEMICONDUCTOR DESIGN



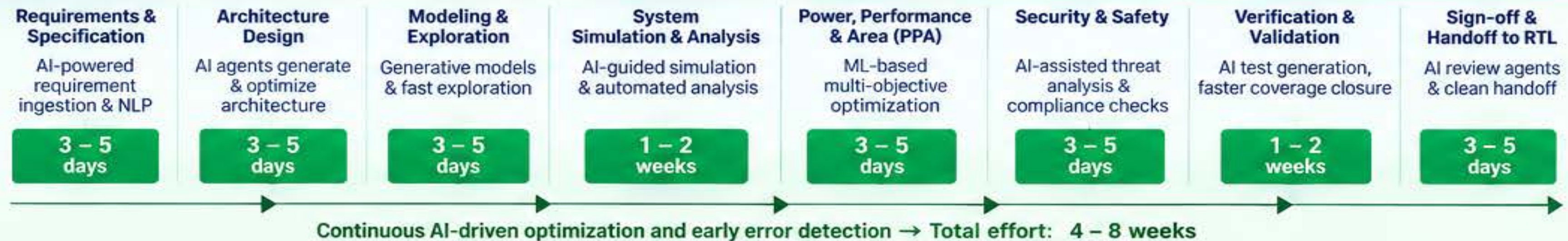
### TRADITIONAL APPROACH – LONG TIMELINE (MANUAL & ITERATIVE)

Total Time: 12 – 24 Months



### AI-POWERED APPROACH WITH PRAGYAN AI (SILICONAI)

Total Time: 4 – 8 Weeks (70–85% Faster)



### EXAMPLE RESULTS (SYSTEM ON CHIP – SOC)



### REAL-WORLD IMPACT



### KEY CHALLENGES (TRADITIONAL)

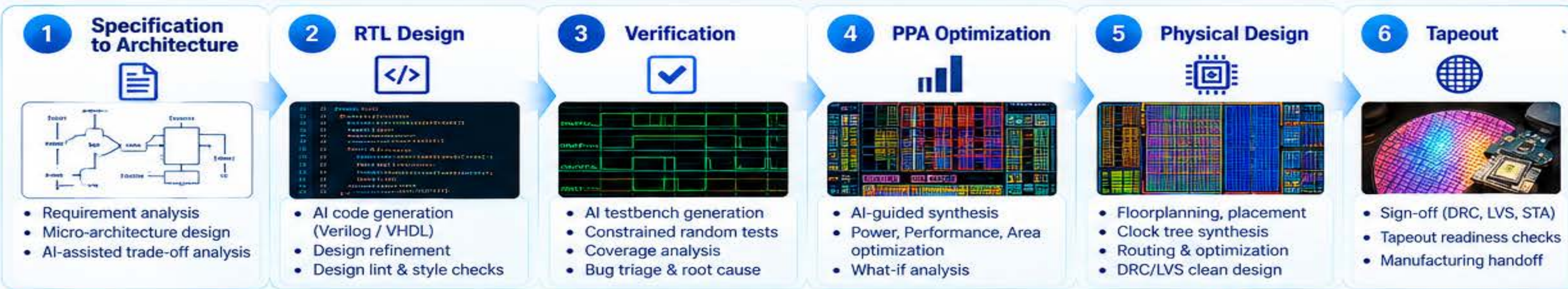


### TIME REDUCTION & PRODUCTIVITY GAIN



### AI SOLUTIONS ACROSS SYSTEM LEVEL TASKS





## CHIP DESIGN CHALLENGES (TRADITIONAL)

- High design complexity (Millions - Billions of gates)
- Long development cycles (12 - 24+ months)
- Need for specialized, scarce expertise
- Multiple iterations due to bugs and PPA issues
- High cost of EDA tools and compute resources
- High risk of schedule slip and tapeout failure

## TRADITIONAL vs AI-POWERED CHIP DESIGN TIMELINE



## IMPROVEMENTS WITH AI

- 70 - 85%** Faster Time-to-Market
- 30 - 50%** Lower Development Cost
- 2 - 5x** Higher Productivity
- Better PPA** (10 - 30% improvement)
- Higher First-Pass Success** (50 - 80% reduction in re-spins)

## BUSINESS IMPACT

- Accelerate product launch and market capture
- Lower NRE and development cost
- Higher design quality, reliability and performance
- Overcome shortage of specialized talent
- Enable complex SoCs with limited engineering resources

## SILICONAI MULTI-AGENT AI OS FOR CHIP DESIGN



## EDA TOOL ECOSYSTEM

synopsys

cadence

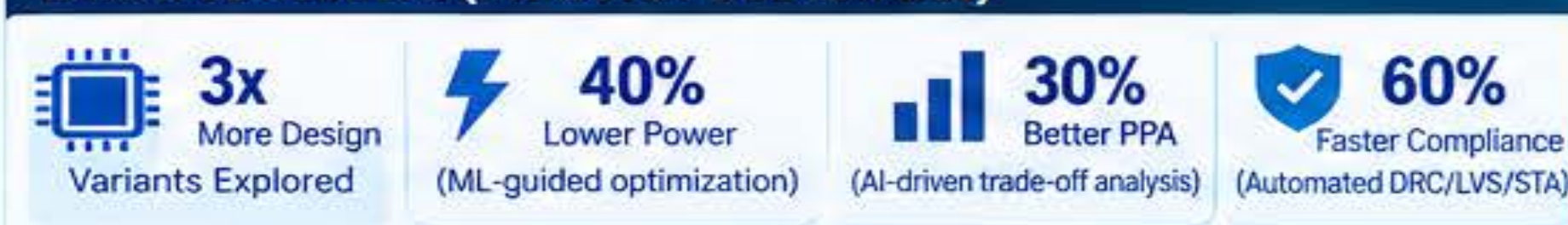
SIEMENS

Ansys

Qualcomm

arm ...

## EXAMPLE RESULTS (INDUSTRY USE CASES)



## CHIP TYPES SUPPORTED



## AI LEARNING LOOP

